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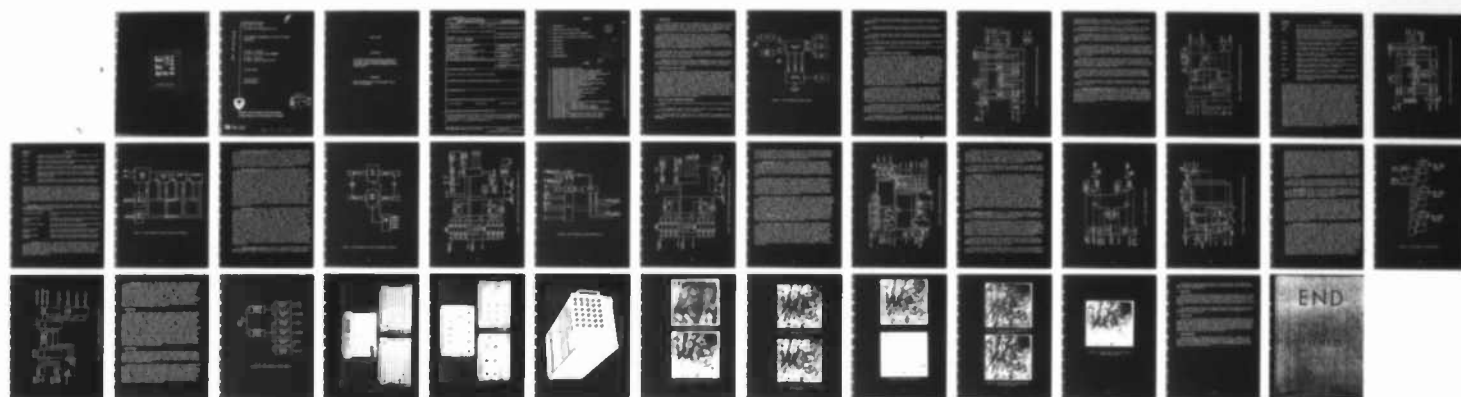
AN AIRBORNE PROGRAMMABLE DIGITAL TO VIDEO CONVERTER(U)
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AN AIRBORNE PROGRAMMABLE DIGITAL TO VIDEO
CONVERTER

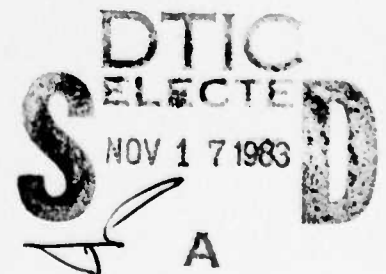
VINCENT J. ORGANIC
US ARMY ELECTRONICS R&D COMMAND

EDWARD A. KARCHER
US ARMY AVIONICS R&D ACTIVITY

OCTOBER 1983

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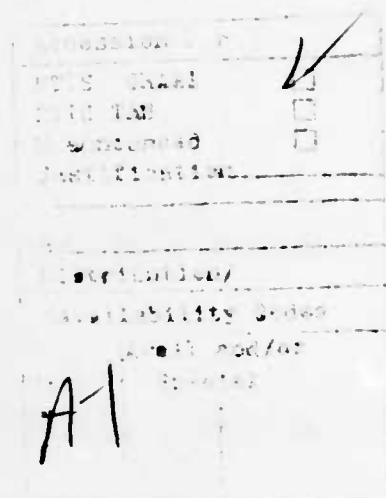
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1. INTRODUCTION

This report describes the design and fabrication of a microprocessor controlled Digital to Video Converter (DVC). The converter accepts and converts data from an external digital computer into a standard 525-line television format which can be displayed in either black and white or color. The system was developed for night navigation/pilotage and nap-of-the-earth helicopter flight studies.

Survivability of Army helicopters under the threat of radar-directed anti-aircraft weapons requires flying at or below tree top level during day and night conditions. The pilot must be aware of the upcoming terrain characteristics. At present, low level operations are performed with the pilot dedicated to the task of piloting the vehicle. Using hand-held maps, the copilot verbally informs the pilot of upcoming terrain. At night, this is extremely difficult. Improving the method of informing the pilot of approaching terrain, and reducing the hazards of low level night flight, are the desired goals of this project.

The design goal was to develop a general purpose computer-driven display whose information content and control functions could be determined by software. Contour maps displaying up to 16 shades of grey or color and various aircraft symbology were the two main items to be displayed.

A companion report entitled "An Airborne Programmable Digital Converter Interface and Operation Manual," Technical Report No. AVRADCOM TR 80-E-4, covers the operational commands, data structure and storage, and interface for the converter.

2. DESCRIPTION OF DISPLAY SYSTEM

Figure 1 is a block diagram of the Airborne Display System showing the location and functional interface of the Digital to Video Converter. The display system is under control of a Singer Kearfott SKC 2000 computer. The computer generates the map data based upon the selected operating program and the aircraft sensor inputs. A typewriter terminal is used as an interface with the system operator for control and status information. Map and alphanumeric data are entered into the converter via the SKC Computer Bus consisting of a 32-line data bus, a 16-line address bus, and a 9-line control bus. The computer can also read data from the converter along with the converter status information. Under computer control, the converter will display the map and alphanumeric data on any combination of the three television monitors shown. Synchronization signals are also supplied to the monitors as well as the other external video sources. The converter will also display or mix with the map data video from up to four external sources, such as a television camera or symbology generation equipment, upon control from the computer.

3. DIGITAL TO VIDEO CONVERTER REQUIREMENTS

The converter is required to perform the following as part of an integrated display system:

- a. Be programmable from an external Singer Kearfott SKC 2000 computer system in both data format and control function selection.
- b. Provide output data compatible with a standard 525-line interlaced raster scan television format, and operate with either 512-by-512 or 256-by-256 pixel/line resolutions.

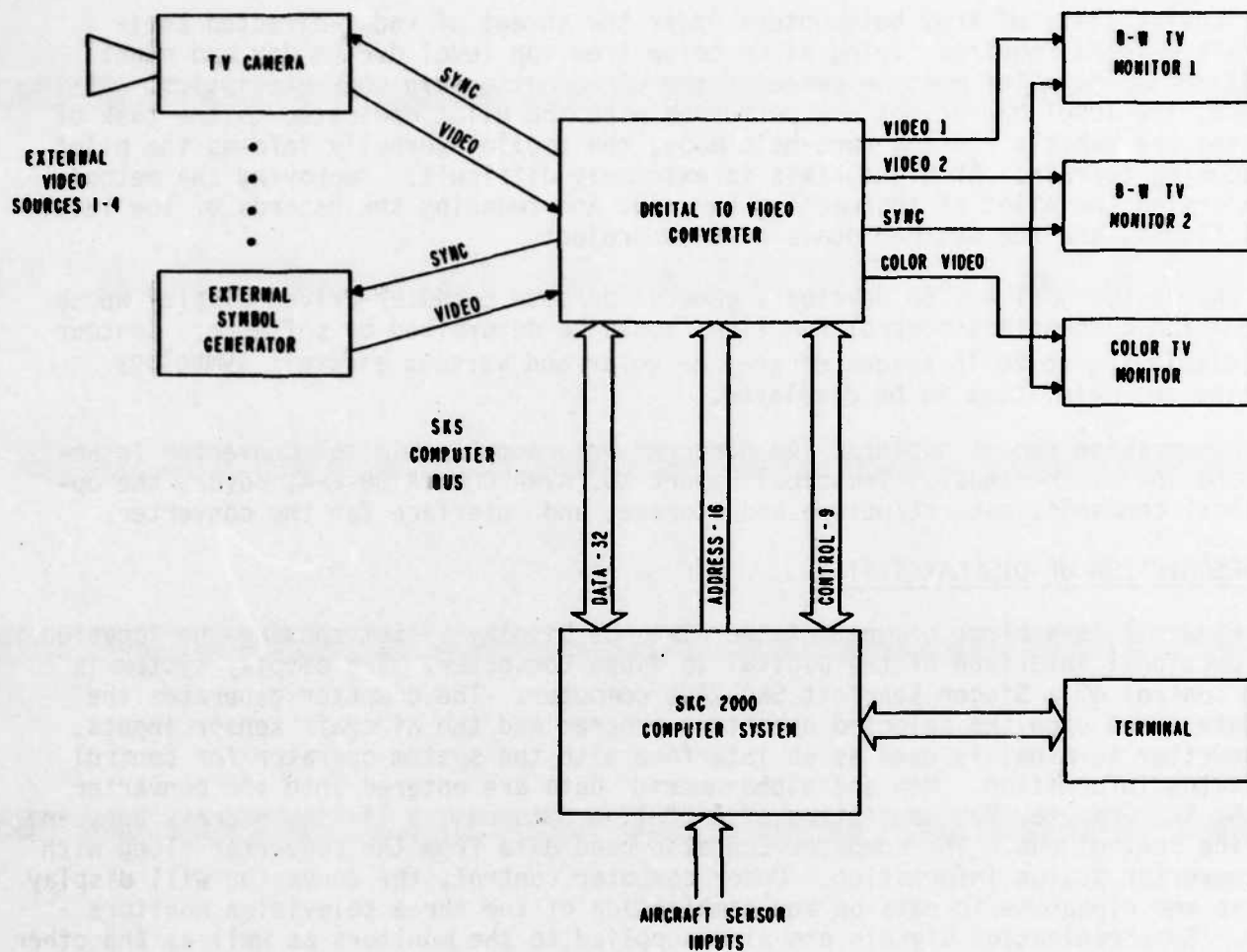


Figure 1. Block Diagram of Display System.

c. Provide storage and operational capability for the display of maps in 16 shades-of-grey or 8 color hues, with superimposed flight symbols, and alphanumeric characters.

d. Allow the display memory to be available to the Singer Kearfott computer for use as a stand-alone auxiliary read/write memory when not in use for display purposes.

e. Provide, under software control, synchronization to external video sources, mix external and internal video signals, and be synchronized from external synchronization sources.

f. Provide output data selection under software control for display on two black and white television monitors and/or a three-gun color television monitor.

g. Be packaged in an approved airborne enclosure and be capable of being flight tested in a helicopter.

4. DESCRIPTION OF THE DIGITAL TO VIDEO CONVERTER

Figure 2 is a simplified block diagram of the DVC. The SKC Computer Bus, consisting of 32 data lines, 16 address lines, and 9 control lines, interfaces the converter with the host computer. The control lines consist of handshake and operational mode signals for controlling the flow of data between the two units. These lines are routed to the Central Processing Unit (CPU) which controls the overall operation of the converter. The CPU contains an 8085 microprocessor to permit versatile programmable operation of the converter. The CPU communicates with the rest of the converter via its own CPU Bus consisting of a data, address, and control structure. A memory for the CPU is located on the CPU Bus and contains the software and data storage for operation of the converter. The data and address lines from the SKC Computer are routed to the SKC Data and Address Interface where they can be connected to the Input Bus data and address lines, respectively, under control of the CPU. In the proper mode, the SKC Computer can read or write from the Display Memories which are also connected to the Input Bus in the converter. This permits the computer to load map, alphanumeric, and symbology data into the Display Memories for future display or utilize these memories for bulk RAM storage.

Five Display Memories are available in the converter. Each memory contains 8K 32-bit words which is sufficient storage capacity to store one-bit level of a 512-pixel/line by 525-line-per-frame raster scan television display. Four of these memories are used to store the map data, thus permitting a 16 shades-of-grey map presentation on a conventional black and white interlaced television monitor. The fifth Display Memory is used for the storage of alphanumeric or flight symbol data which is only displayed in a black and white format. This data can be entered from the computer or can be locally generated by the converter CPU.

The Input Bus Memory Controller provides two functions. The first is to generate the necessary timing and interface signals for the Display Memories when they are accessed by either the SKC Computer or CPU via the Input Bus. The second is to provide an 8-bit to 32-bit data bus interface along with an address interface to permit the CPU to access the Display Memories.

The Display Memories also have an additional port to the Display Bus. The Display Bus is primarily used by the Map Generator to read data from the Display Memories for display. The CPU determines the bus, Input or Display, to which each of the five

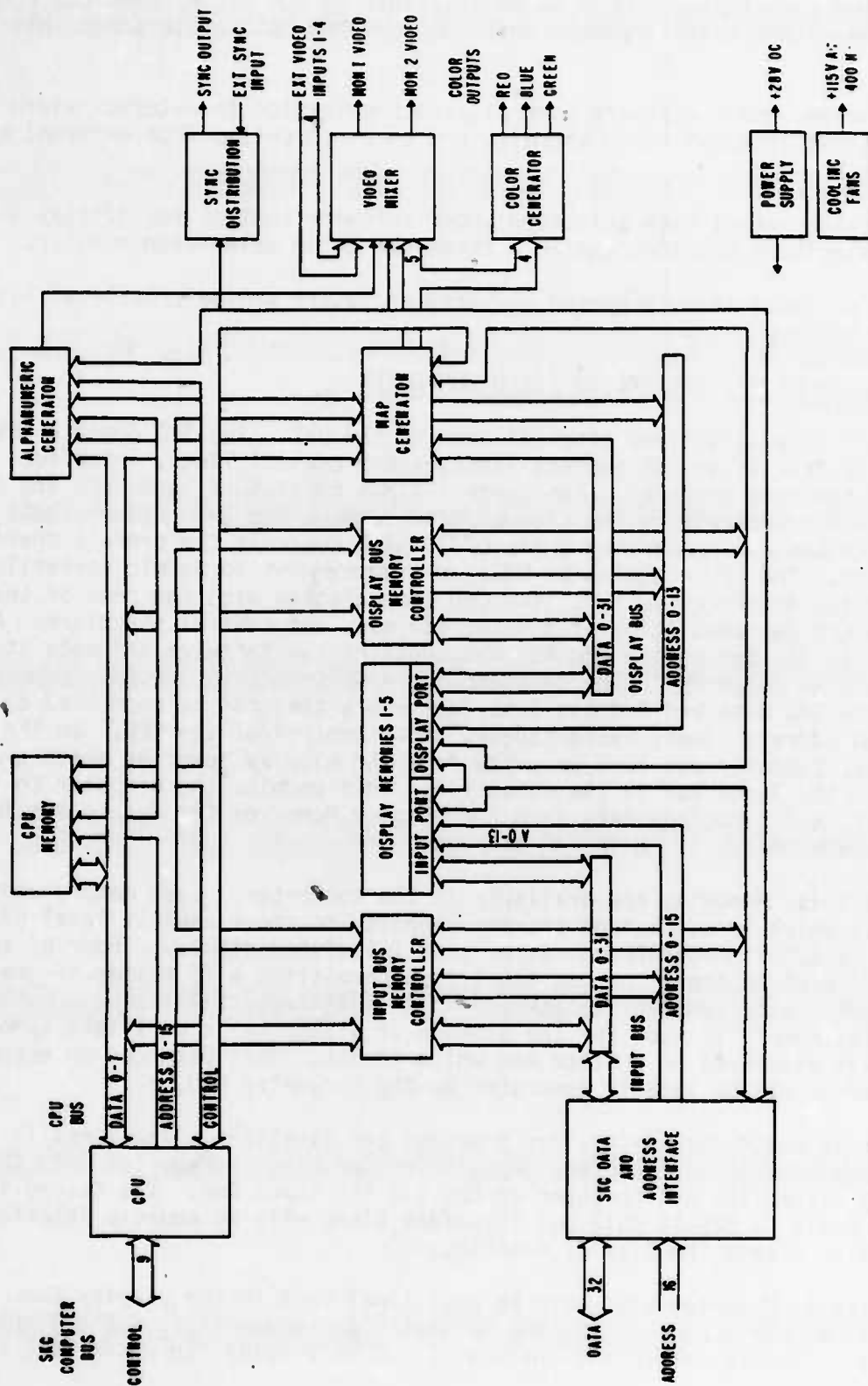


Figure 2. Simplified Block Diagram of Digital to Video Converter.

individual Display Memories is connected. Thus, it is possible to have some of the Display Memories utilized for display while the balance of the memories are being addressed by the SKC Computer or CPU for the loading of new data.

The Display Bus Memory Controller functions in a similar fashion to the Input Bus Controller except that it provides timing, data, and address access functions for the CPU and Map Generator for access of Display Memories via the Display Bus.

The Map Generator reads data from the Display Memories, formats the data, and provides the necessary timing signals for the display of maps and symbology on a television monitor. The Map Generator contains a programmable cathode ray tube (CRT) controller which is accessed by the CPU to permit operation in a wide variety of modes.

The Alphanumeric Generator permits the converter to display alphanumeric messages on the television monitors. These messages can be generated by the CPU or entered from the SKC Computer to the Display Memories where they are accessed by the CPU for display via the Alphanumeric Generator. The outputs from the Alphanumeric and Map Generators are fed to the Video Mixer for transmission to two black and white television monitors for display.

The Video Mixer is also under program control of the CPU for selection of the converter output video and optional mixing of the converter video with up to four external video signals. The output of the Map Generator is also fed to the Color Generator which converts the map and symbology data into red, blue, and green color monitor drive signals for optional display in color.

The Sync Distribution circuitry provides standard television synchronization signals for use internal to the converter and distribution to external equipment. This circuitry, under CPU control, can also receive sync signals from an external source for subsequent synchronization of the converter and distribution to external equipment.

The Power Supply provides all necessary operating potentials for the converter circuitry. Each function in the converter is described in detail in subparagraphs a through l below.

a. Central Processing Unit (CPU) (Figure 3). The CPU functions to provide overall control over the DVC and to communicate with the SKC computer. The heart of the CPU is an 8085 microprocessor manufactured by Intel which provides programmable control over all operations. The clock signal, CLK 5.0/, is derived from the Input Bus Memory Controller and is used as the master clock for the CPU. The nine twisted wire pairs are the control signals between the host SKC computer and the DVC to permit the SKC to direct and monitor the operation of the DVC. These signals perform the following functions:

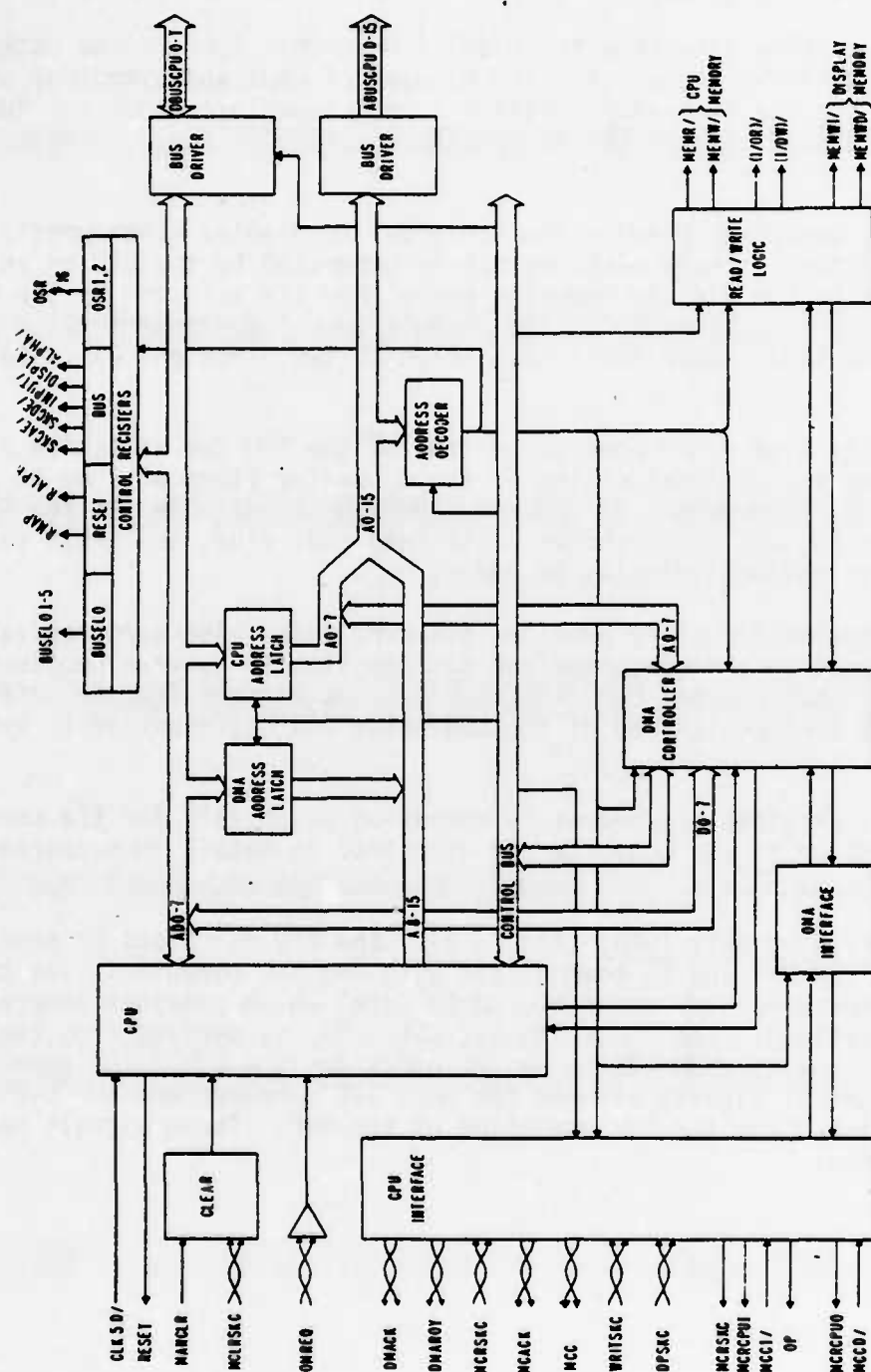


Figure 3. Simplified Block Diagram of Central Processing Unit.

<u>MNEMONIC</u>	<u>DESCRIPTION</u>
MCLRSKC	Master clear from the SKC, clears all circuitry in the DVC.
OMREQ	Operational Mode Request from the SKC, indicates that the SKC is requesting a change in the operational mode of the DVC. This signal sets an interrupt request to the DVC CPU which will be serviced by the CPU when the present operating routine can be interrupted. The CPU will then fetch and execute the instruction specified by the Control Words stored in Display Memory 1 by the SKC.
OMACK	Operational Mode Acknowledge from the DVC, indicates to the SKC that an OMREQ has been received and is being serviced.
DMARDY	Direct Memory Access (DMA) Ready from the DVC, indicates to the SKC that the DVC is ready for a DMA operation.
MCRSKC	Memory Cycle Request from the SKC, indicates the SKC is requesting access of the DVC Display Memory.
MCAACK	Memory Cycle Acknowledge from the DVC, indicates to the SKC that a requested access of the Display Memory is in progress.
MCC	Memory Cycle Complete from the DVC, indicates to the SKC that a requested access of the Display Memory is complete.
WRITSKC	Memory Write Command from the SKC, determines if the Display Memory cycle requested is in the read or write mode.
DPSKC	Data Processed from the SKC, indicates to the DVC that the data from the DVC has been accepted by the SKC after a Display Memory read access is complete.

The remaining six control lines from the CPU interface form part of the DVC Control Bus and are used in the access of the Display Memories. The 8085 CPU has an 8-line multiplexed address/data bus (AD 0-7) for the lower 8 bits of the address and the 8-bit data bus. During a memory or Input/Output (I/O) access cycle, the lower 8 bits of the address first appear on the bus and are latched in the CPU address latch. These 8 lines combined with the 8-line address bus (A8-15) form the complete 16-line address which flows through the bus driver to the CPU Address Bus, ABUSCPU 0-15. During the data transfer part of the access cycle, data flows in a bidirectional manner on the AD 0-7 bus depending upon whether a read or a write cycle is in progress. This data flows through the bidirectional bus driver to the CPU Data Bus, DPUSCPU 0-7. The 8085 CPU also incorporates a control bus for controlling the overall circuit operation. Some of the control lines operate the read/write logic which outputs the necessary read/write commands for access of the CPU Memory, I/O devices, or Display Memories. A set of five control registers outputs various control commands to the DVC Control Bus from the CPU. The BUSELD register determines which of the five Display Memories are placed on the Input Bus; the balance are placed on the Display Bus. The RESET register permits the Map and Alphanumeric Generator logic circuitry to be reset by CPU software through the RMAP and RALPHA commands, respectively. The Bus register allows the CPU to control the operation of the various bus drivers located within the DVC to permit CPU and SKC Computer access to the Display Memories via the Input Bus, CPU access to the Display Memories via the Display Bus, and CPU access to the Alphanumeric Generator. The bus configuration drawing is shown in Figure 4. The bus control signals operate as follows:

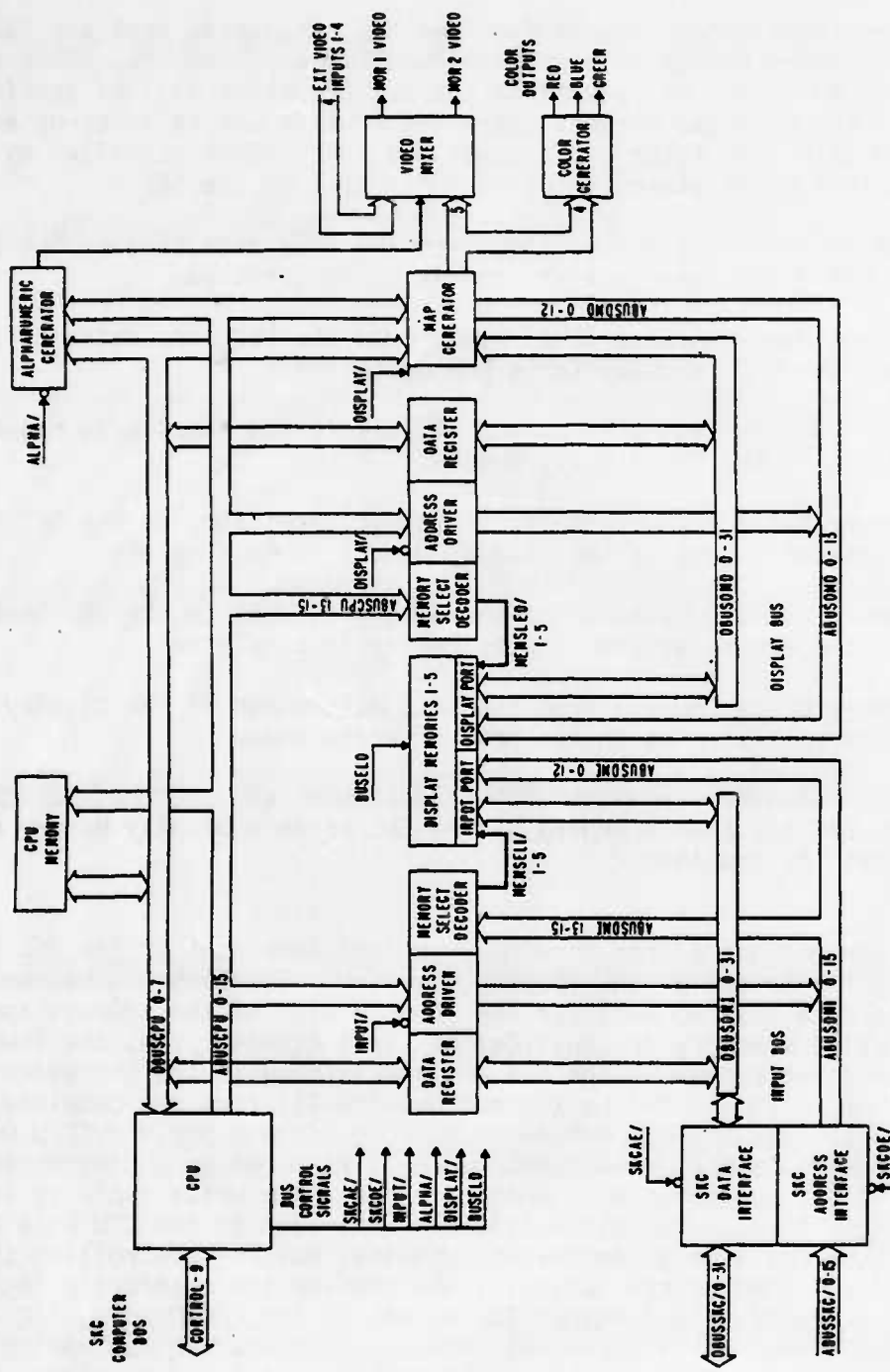


Figure 4. Simplified Block Diagram of Data and Address Bus Configuration.

MNEMONICDESCRIPTION

SKCDE/	Enables the SKC Data Interface to permit the SKC Computer to have access to the Input Data Bus, DBUSDMI.
SKCAE/	Enables the SKC Address Interface to permit the SKC Computer to have access to the Input Address Bus, ABUSDMI.
INPUT/	Enables the Address bus driver on the Input Bus Memory Controller to permit the CPU to have access to the Input Address Bus, ABUSDMI.
ALPHA/	Enables the CPU Data and Address bus drivers to the Alphanumeric Generator to permit the CPU to write data into the Alphanumeric Generator page memory.
Display/	Enables the address bus driver on the Display Memory Controller to permit the CPU to have access to the Display Address Bus, ABUSDMD.

The Operational Status Registers 1&2 (OSR 1&2) are used for diagnostic purposes to determine the functional status of the CPU. The output of these registers is periodically updated as a function of the present CPU operating routine and is fed to a status plug on the CPU where a logic analyzer can be connected to monitor the operational status. There is also a DMA controller in the CPU. An 8257 programmable DMA controller circuit manufactured by Intel was used for this application. The DMA controller is used for two functions, to permit rapid clearing of the Display Memories by the CPU and the block transfer of data from the SKC Computer to the Display Memories.

CPU Software. The CPU software will only be summarized in this report. The following programs were written in assembly language for an Intel Corporation Intellect Microcomputer Development System.

Initialization Program	Initializes the DVC upon power turn-on or clearing of the DVC.
Operational Polling Program	Determines the operational mode of the DVC based upon data received from the SKC Computer.
Display Turn-on Program	Turns on the display in the proper operating mode based upon data received from the SKC Computer.
Display Turn-off Program	Turns off the display and performs control and Display Memory initialization directed by the SKC Computer.
Alphanumeric Page Program	Transfers data from the Display Memories to the Alphanumeric Generator page memory for prompting messages.

b. CPU Memory (Figure 5). The CPU Memory stores software and data for use by the CPU in the operation of the converter. The CPU accesses the memory via the CPU Data and Address bus under two control signals. The memory consists of 1K of static RAM and 6K of EPROM. Three ultraviolet erasable 2K by 8-bit wide EPROM ICs were used in the design to expedite software modifications. The memory select logic selects the proper memory circuit and access mode in accordance with the address and control signals, respectively.

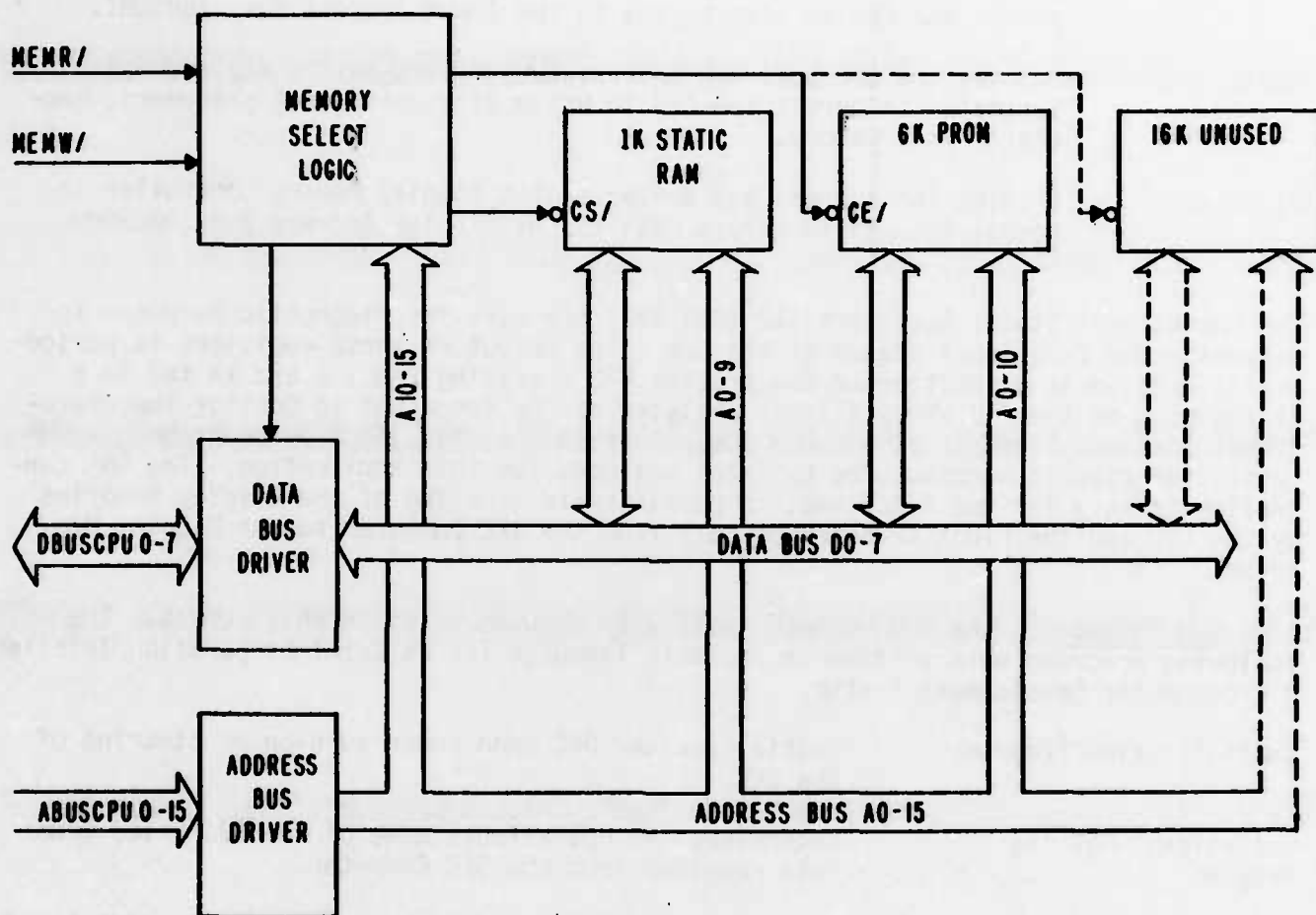


Figure 5. Block Diagram of Central Processing Unit Memory.

c. SKC Data and Address Interface (Figure 6). The SKC Data and Address Interface provides driver buffering between the SKC Computer Bus and the converter Input Bus. A bidirectional three-state bus driver is used on each of the 32 data lines. A unidirectional bus driver is used on each of the 16 address lines. Appropriate enable logic is also located on this card and is controlled by the converter CPU. The circuitry permits data to be read or written from the computer to the Display Memory at the address location determined by the computer. The three-state capability of the bus drivers also permits the computer to be disconnected from the converter Input Bus when the converter is busy performing a processing function.

d. Input Bus Memory Controller (Figure 7). The Input Bus Memory Controller provides the interface/control circuitry for operation of the dynamic RAM based Display Memories when accessed via the Input Bus either by the SKC Computer or the converter CPU. There is also a bidirectional 8- to 32-bit data converter and address bus driver required for CPU access of the Display Memories through the Input Bus. The upper right portion of the diagram contains the circuitry utilized in the memory interface/control function. This circuitry provides the system clock signals, memory refresh timing, arbitration between refresh, SKC Computer, and CPU access requests, and necessary handshake commands. The left portion of the drawing shows the 8- to 32-bit data converter. There are separate read and write registers to permit bidirectional CPU access of the Display Memories. When the CPU is accessing the Display Memories, the CPU Address Bus is connected to the Input Address Bus via the bus driver shown in the drawing. The desired memory is selected by the memory board decoder based upon the supplied address. In the read mode, data in a 32-bit format is read from the selected memory via the Input Data Bus to the read register. The contents of the read register are then read by the CPU in four successive 8-bit bytes via the CPU Data Bus. In the write mode, the CPU writes four 8-bit bytes into the write register via the CPU Data Bus. The contents of the write register are then written into the Display Memory in a 32-bit format at the address location present on the CPU Address Bus.

e. Display Memories (Figure 8). Five Display Memories are utilized in the converter. Four are used for the storage of map data to permit the display of maps in 16 brightness levels or shades-of-grey. The fifth is used for the storage of flight symbology or alphanumeric data. Each Display Memory contains thirty-two 8K-bit dynamic RAM integrated circuits. This is sufficient storage for one bit level of a 512-pixel-by-525-line television display. Each memory is organized as a two part design with one part connected to the Input Bus and the second part to the Display Bus. Control signals from the CPU are routed to the memory cycle and refresh timing circuitry, and are used to determine which bus the memory is connected to. This architecture was chosen to permit the CPU to have control over the use of the memories. Thus, some of the memories can be placed on the Display Bus for the display of maps or symbology and the balance placed on the Input Bus for updating by the SKC Computer or CPU. The portion of each Display Memory not utilized for display purposes is available to the SKC Computer for the storage of DVC control words and prompting messages for display. The SKC Computer writes control words into predetermined locations in the memory which are read and interpreted by the CPU as instructions to perform the new task when directed by the SKC Computer via an Operational Mode Request (OMREQ) signal. In a similar fashion, prompting messages can be read from the non-displayed portion of the memories by the CPU and written into the Alphanumeric Generator for display.

f. Display Bus Memory Controller (Figure 9). The Display Bus Memory Controller performs a function similar to that of the Input Bus Memory Controller except that this controller is used for the Display Bus. This controller is somewhat simpler

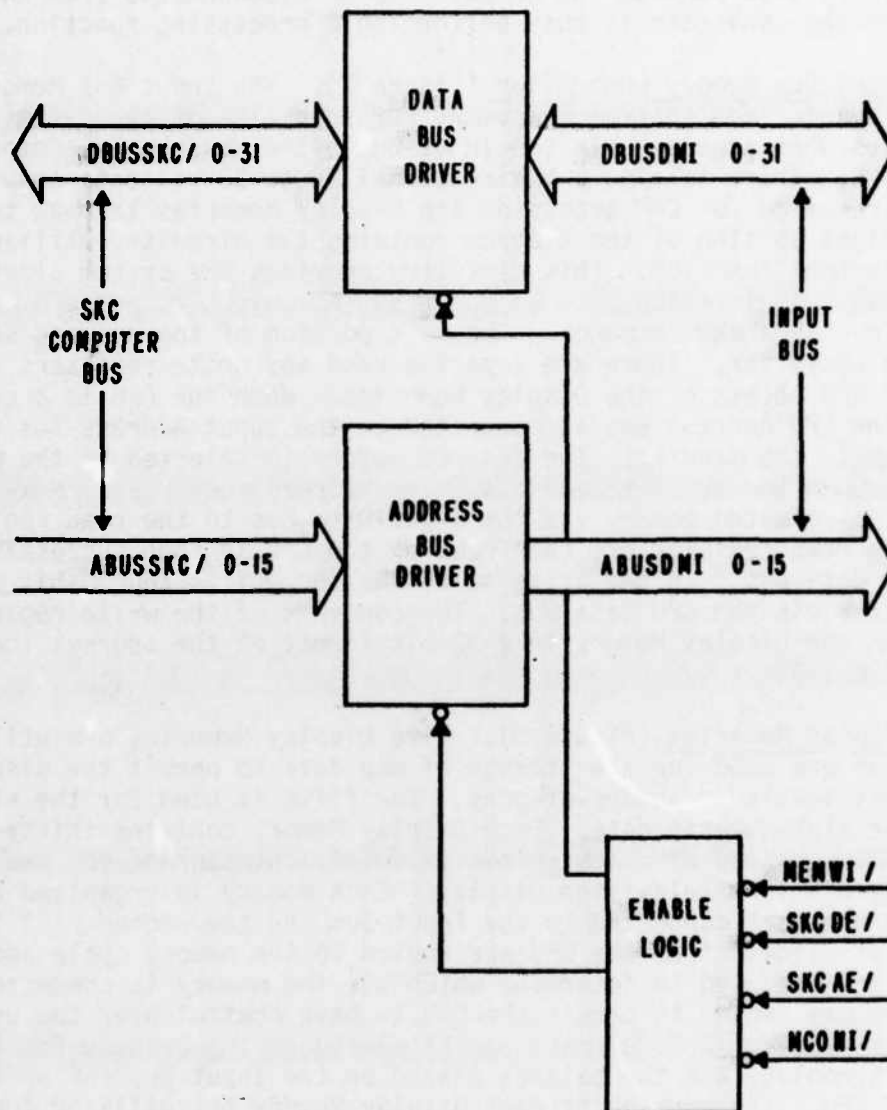


Figure 6. Block Diagram of SKC Data and Address Interface.

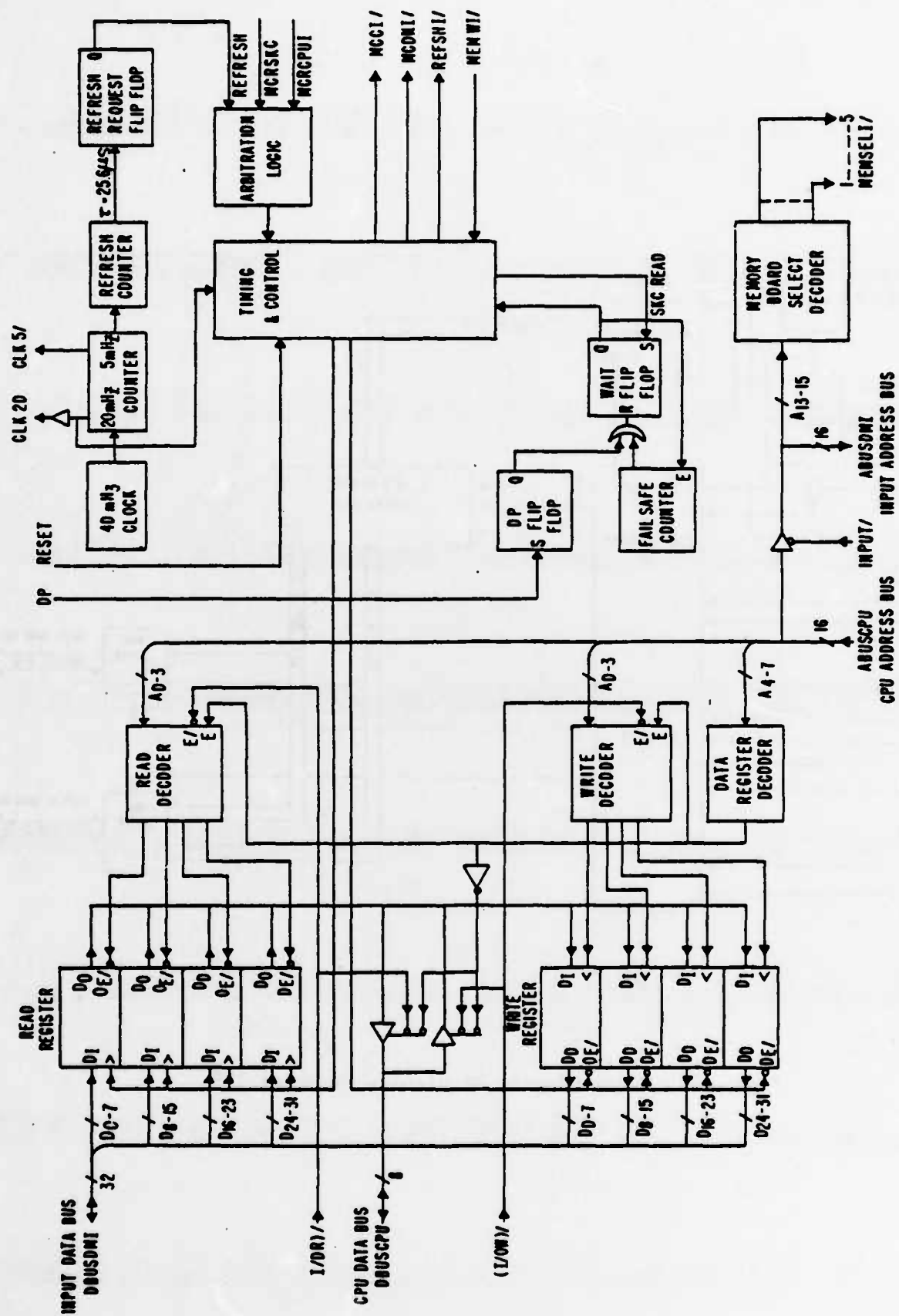


Figure 7. Simplified Block Diagram of Input Bus Memory Controller.

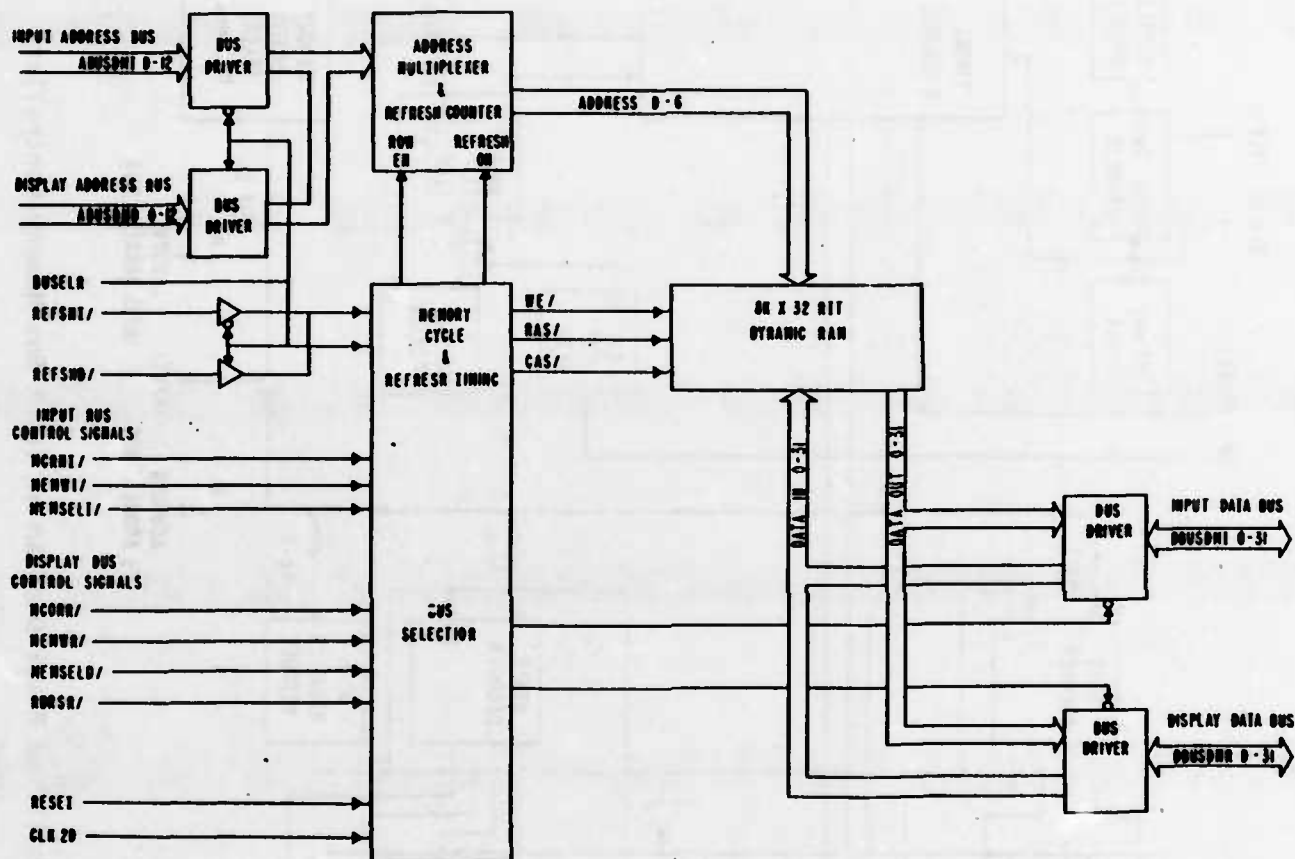


Figure 8. Block Diagram of Display Memories 1-5.

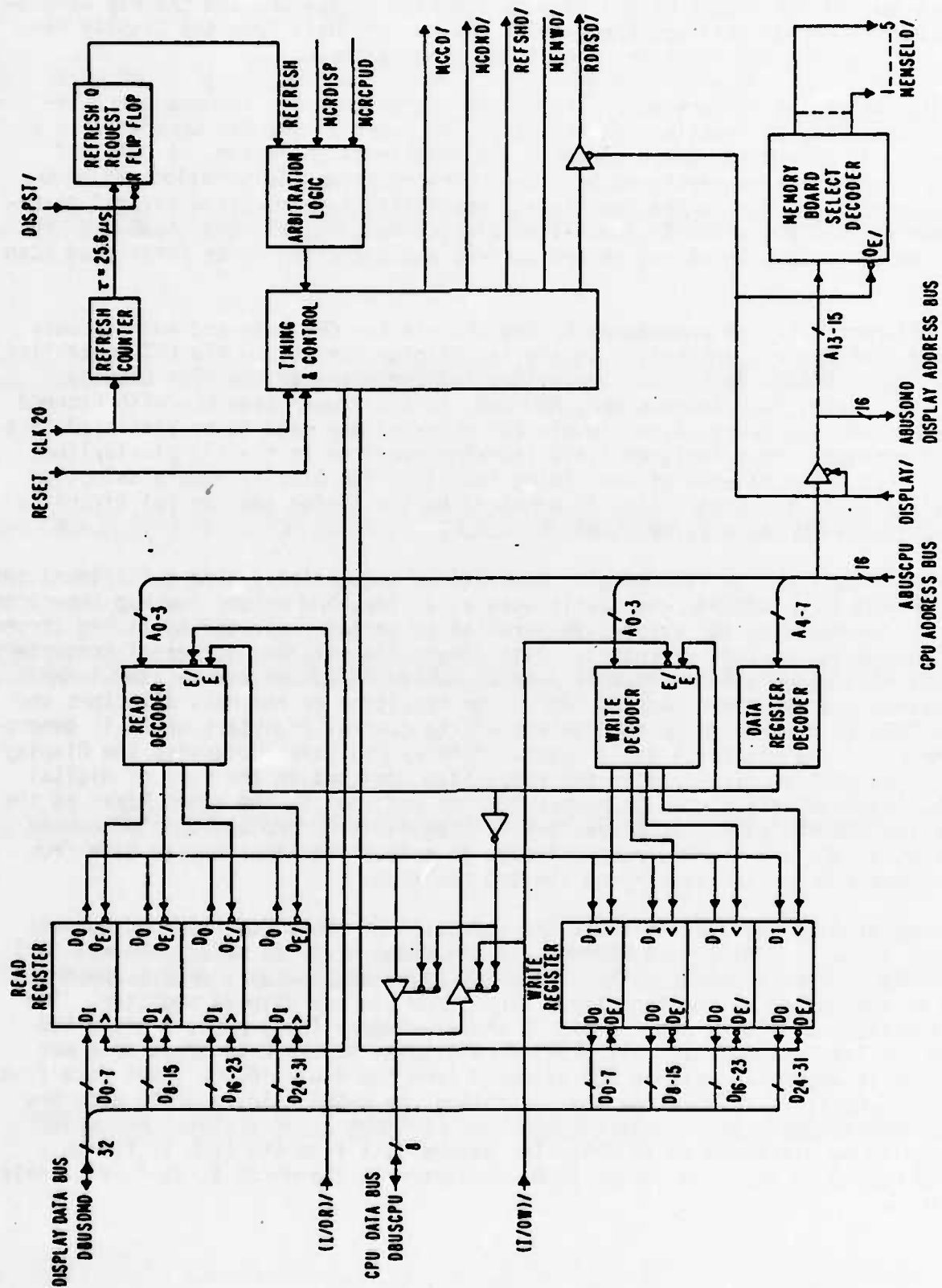


Figure 9. Simplified Block Diagram of Display Bus Memory Controller.

than the Input Bus Memory Controller because there is no provision for SKC Computer access of the Display Bus or clock generation circuitry. The controller performs all functions required for access of the Display Memories by the CPU and the Map Generator. The Map Generator utilizes the Display Bus to read data from the Display Memories to its own internal registers for video presentation.

g. Map Generator (Figure 10). The Map Generator controls the map presentations and other Display functions in the DVC. The heart of the Map Generator is a programmable CRT controller which controls the functional operation. A CRT 5027 Video Timer-Controller manufactured by Standard Microsystems Corporation was used as the CRT controller due to its functional versatility in supporting several operational modes; i.e., 256 and 512 pixels/line display resolutions, the capability to move the map to various locations on the screen, and operation in an interlaced scan mode.

The CRT controller is programmed by the CPU via the CPU Data and Address bus, DPUSCPU and ABUSCPU, respectively. In the map display operation, the CRT controller and associated synchronization logic provides the addresses to the five Display Memories over the Display Address Bus, ABUSDMD, in the proper sequence with respect to the television synchronization signals for accessed map data to be displayed on a television monitor. This includes field indexing required in the 512 pixels/line resolution mode. The balance of the timing functions for Display Memory selection and overall circuit synchronization is provided by the timing and control circuitry which is driven from the display clock, CLK 27.72.

The map data from the five Display Memories is sequentially time multiplexed onto the Display Data Bus, DBUSDMD, one 32-bit word at a time, and enters the Map Generator where it is latched into the respective parallel to serial converter by timing strobes from the timing and control circuitry. Data leaves the parallel to serial converters in a serial fashion on a 5-line serial data bus where it enters the monitor 1 and 2 data selectors and the video mapping PROM. The operation of the data selectors and the video PROM is determined by the content of the control registers which is generated by the CPU. The monitor 1 and 2 digital display registers determine the Display Memories which will be displayed on the respective monitors in the form of digital data. The selected data is fed to output buffers and sent to the Video Mixer as the MON1DIDA/ and MON2DIDA/ signals, respectively. Each digital display register has an output line, ALPHA1 and ALPHA2, respectively, to select the alphanumeric data from the Alphanumeric Generator display on the two monitors.

The map display register controls the operation of the video PROM and outputs two control signals, MON1MAP and MON2MAP, to the Video Mixer to select the monitors that will display the map data. The video PROM operates as a data mapper whose function is controlled by the four input lines from the map display register. The mapping functions available are: 4-bit 16 shades-of-grey (SOG) maps, 3-bit 8-SOG maps with the least significant bit (LSB) from Display Memory 2 ignored, or a map presentation in any consecutive 8 SOG selected from the 4-bit 16-SOG input data from the Display Memories. This latter mode is called the 8-SOG sliding scale mode and is used to permit increased contrast range over portions of a displayed map which would normally be displayed in 16 SOG. The mapped data from the PROM is fed to a buffer and routed to the Video Mixer (D/A) converter as the MAPDA 1, 2, 4, 8 signals, respectively.

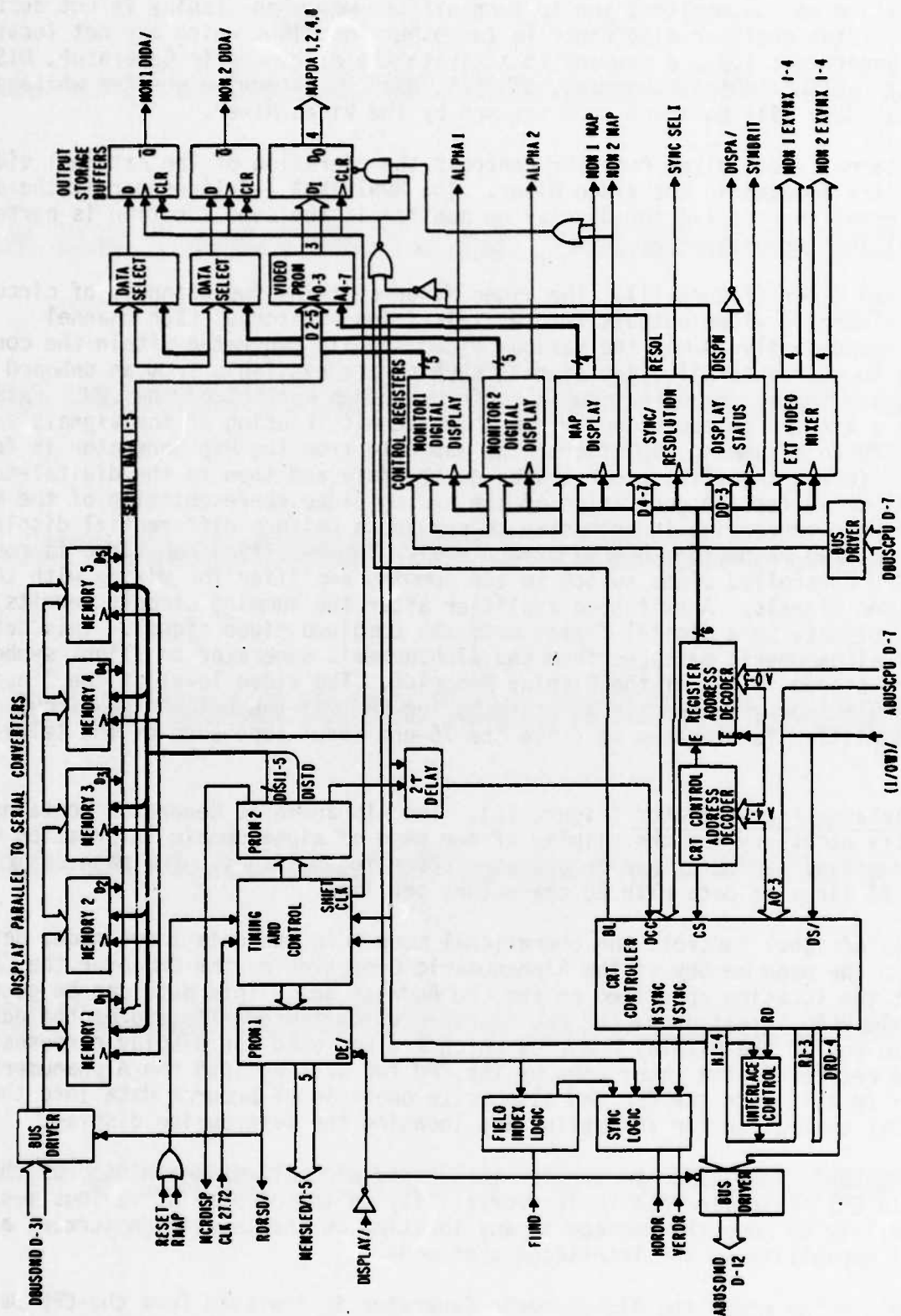


Figure 10. Simplified Block Diagram of Map Generator.

The blanking signal and DISPM display map control signal from the display status register are applied to the output buffer circuitry to display the map in the desired location on the monitors and to turn off the map when display is not desired. The display status register also controls two other functions which are not located on the Map Generator; i.e., a command to activate the Alphanumeric Generator, DISPA/, and a digital data brightness command, SYMBRIT, used to determine whether white or black digital data will be inset onto the map by the Video Mixer.

The external video mixer register controls the operation of the external video mixer circuitry located in the Video Mixer. The MONIEXVMX 1-4 lines permit the selection of external sources 1-4 for display on monitor 1; the same function is performed by MON2EXVMX 1-4 for monitor 2.

h. Video Mixer (Figure 11). The Video Mixer contains two channels of circuitry to provide alternate video outputs for two television monitors. Each channel functions independently to mix the various video signals generated within the converter with up to four external video signals such as are available from an onboard television camera. The mixing operation is performed under control of the CPU. External video signals are fed to the video switch which permits routing of the signals selected by the CPU to a summing amplifier. The map data from the Map Generator is fed to a PROM to perform a logarithmic conversion of the data and then to the digital-to-analog (D/A) converter for generation of the analog video representation of the map. This logarithmic conversion is necessary to provide a uniform differential display brightness between each video quantization level. The resulting map video is routed through a CPU controlled video switch to the summing amplifier for mixing with the external video signals. A switching amplifier after the summing circuit permits "insetting" of data in a digital format onto the combined video signal. This data consists of alphanumeric messages from the Alphanumeric Generator or flight symbology map contours stored in one of the Display Memories. The video level of the "inset" data can be black or white and is selected by the CPU via the brightness circuitry. An output amplifier is provided to drive the 75-ohm input impedance of the television monitor.

i. Alphanumeric Generator (Figure 12). The Alphanumeric Generator contains the circuitry necessary for the display of one page of alphanumeric information which generally contains map notations or operator prompting messages. The page can contain up to 25 lines of data with 80 characters per line.

The DISPA/signal controls the operational mode. In the data input mode, data is written into the page memory of the Alphanumeric Generator by the CPU over the CPU Data Bus at the location specified on the CPU Address Bus. This data can be generated either by the CPU itself or by the SKC Computer which temporarily stores the data in locations in any of the Display Memories which are not used for display purposes; the data may be retrieved at a later time by the CPU for writing into the Alphanumeric Generator. In this mode the CPU can also write operational program data into the programmable CRT controller for formatting and locating the data during display.

The CRT 5027 Video Timer-Controller integrated circuit was again used as the programmable CRT controller due to its versatility in the display of various message lengths, ability to move the message to any location on the television screen, and operational capability in the interlaced scan mode.

In the display mode, the Alphanumeric Generator is isolated from the CPU Data and Address Bus, and its operation is turned over to the CRT controller which reads the page memory in the proper sequence for display on a television monitor in synchronism

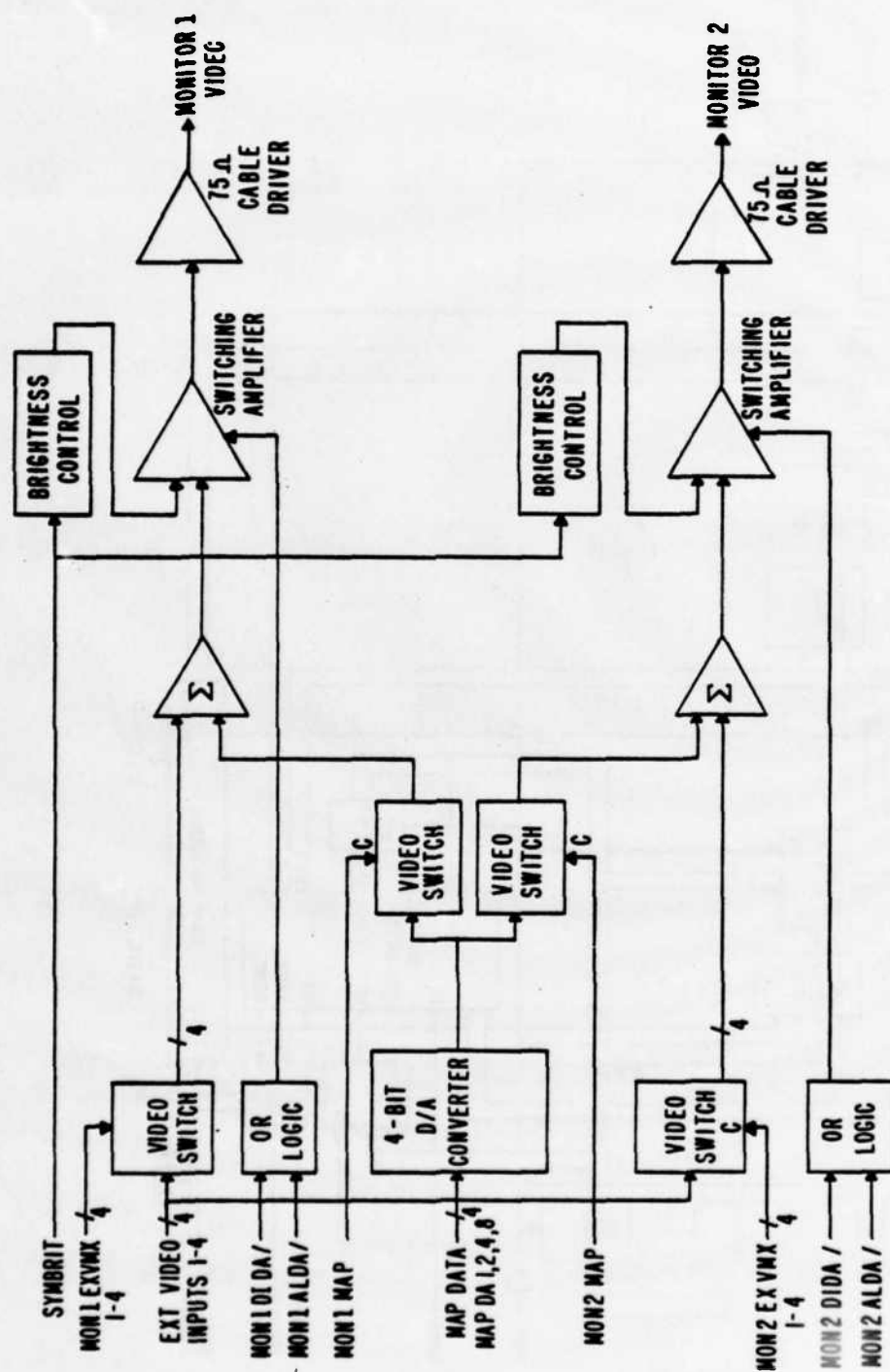


Figure 11. Block Diagram of Video Mixer.

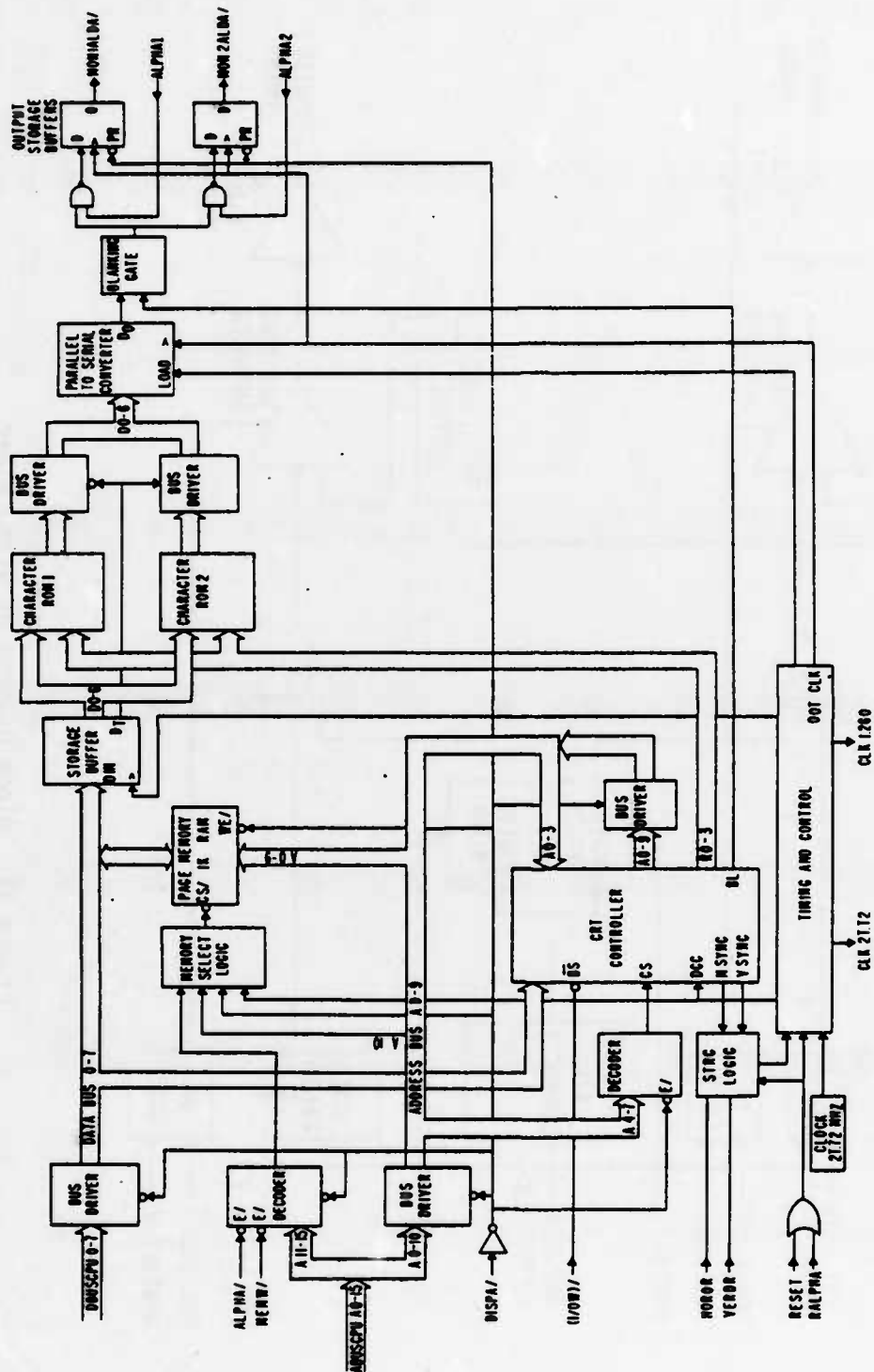


Figure 12. Simplified Block Diagram of Alphanumeric Generator.

with the television synchronization signals. The data from the page memory goes to a storage buffer where it forms part of the address to two character ROMs used to generate the dot matrix pattern for the character being displayed. The balance of the address comes from the CRT controller to permit scanning of the character dot matrix in synchronism with television sync signals. A total of 256 characteristics are available from the ROMs, including upper and lower case letters, numbers, and special symbols. The character ROM to be displayed is selected by bit 7 of the address which permits routing of the dot display data to the parallel to serial converter for conversion to a serial format required for raster scan display. The output of the converter is fed to the blanking gate where a logic and function is performed with the blanking signal to permit the display of data on only the desired portion of the television raster. The output section consists of a storage buffer for each of the two respective alphanumeric outputs for monitor 1, MON1ALDA/, and monitor 2, MON2ALDA/.

Two control signals, ALPHA1 and ALPHA2, determine which monitors will display the data. A 27.72-MHz clock drives the timing and control circuitry. All of the display function timing throughout the entire DVC is derived from this clock including the internal synchronization circuitry which operates from the CLK 1.260 signal.

j. Color Generator (Figure 13). The Color Generator accepts the three bit map data and generates red, blue, and green drive signals for presentation of the map on a color television monitor. Eight color intensity levels/hues are available from the Color Generator for map display along with one additional level used for inseting map contours, symbology, or alphanumeric data.

In operation, the Color Generator enters the three-bit map data into a decoder which decodes the data into eight mutually exclusive outputs. Each of the decoder outputs feed three potentiometers which set the red, blue, and green color intensity levels. The relative amplitude of each primary color determines the hue of the composite output color. Thus, each decoder output represents one intensity level/hue which can be chosen by adjusting the three associated potentiometers. The outputs of each red, blue, and green potentiometer are summed into respective 75-ohm cable driver amplifiers which feed a three-gun color monitor. In addition, the data from one Display Memory, MON1DIDA/, is fed to a circuit which inserts the data into the color map. This memory usually contains map contour, symbology, or alphanumeric data which is displayed on the map. Separate potentiometers are used to set the level/hue of the inset data.

k. Synchronization Generator (Figure 14). This board provides synchronization for internal circuitry and furnishes television synchronization signals for distribution to up to five external video users. The board has its own sync generator for use when the converter is the master sync distribution center for the display system. The clock signal for the sync generator is derived from the converter master clock to maintain synchronization with the rest of the converter functions. Synchronization signals can also be provided from an external master source. External sync signals at either the standard EIA or TTL levels are accepted depending upon the setting of the sync level multiplexer. This setting is hardwired at the board level. In the external synchronization mode, an odd/even field index is generated for internal use by the converter in the 512 pixel/line display mode. A control signal supplied by the CPU, SYNCSELI, switches the output multiplexer between internal or external sync signals to permit programmable control of the sync source. The upper set of output drivers provide synchronization, HORDR, VERDR, FIINO, at TTL levels to other sections of the converter. The output level shifters shift the level of the sync signals to EIA levels and provide five 75-ohm drivers for each signal; i.e., horizontal drive, vertical drive, and composite sync for external distribution.

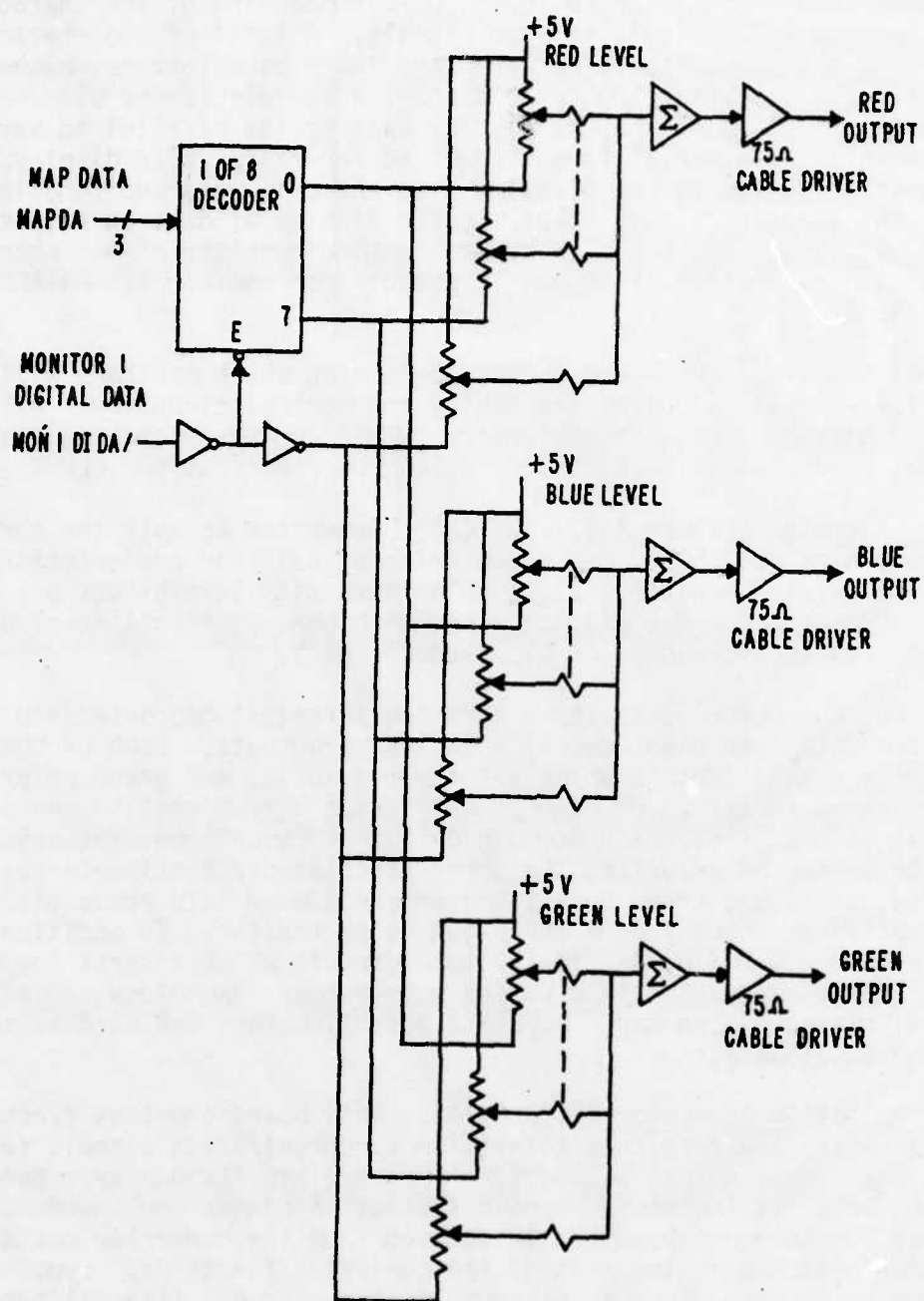


Figure 13. Block Diagram of Color Generator.

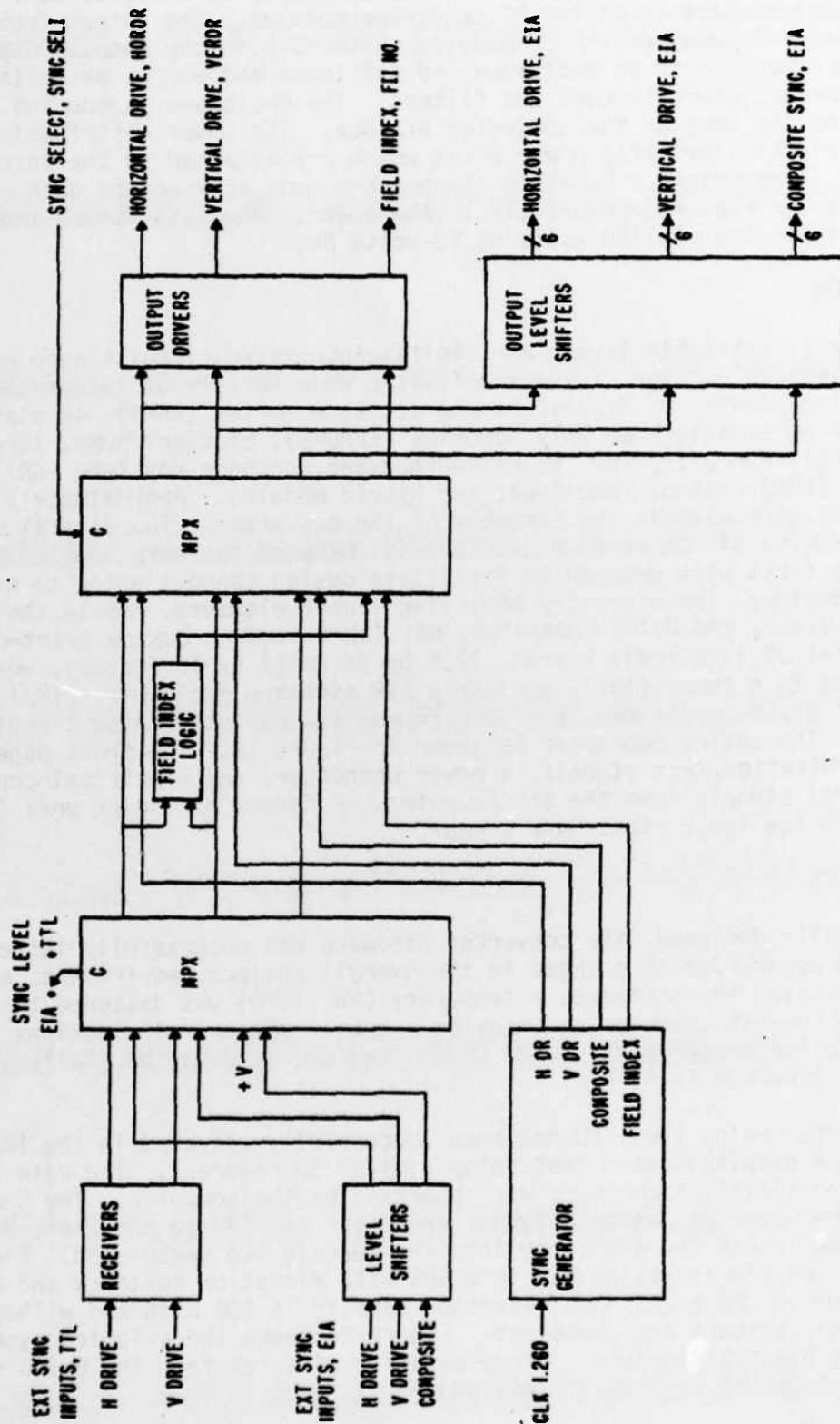


Figure 14. Block Diagram of Synchronization Distribution.

1. Power Supply (Figure 15). The Power Supply supplies all necessary operating potentials required for operation of the converter circuitry. The supply is modular in construction consisting of a number of power modules manufactured by Power Cube Corporation. The prime power input to the Power Supply is 28-volts DC from the aircraft power system which feeds two AC converter modules. The output from each AC converter feeds the power converter modules which furnish the output DC potentials. All modules are mounted in an enclosure and all input and output potentials are routed into the enclosure through EMI filters. The enclosure is mounted on a heat sink located on the back of the converter ATR box. The power distribution within the converter is via two laminated power buses which are attached to the interconnection circuit card. Appropriate taps along the bus are made adjacent to each circuit board to route the required potentials to the board. The total power input to the converter is approximately 160 watts at 28-volts DC.

5. FABRICATION

Commercially available linear and digital integrated circuits were used in each circuit board assembly. The circuits reflect a wide variety of integrated electronic technologies including: 8K dynamic random access memories (RAMs), 4K static RAMs, Electrically Programmable Read Only Memories (EPROMs), bipolar PROMs, large scale integration (LSI) circuitry for the microprocessor, cathode ray tube (CRT) and direct memory access (DMA) control functions, and hybrid modules. Approximately 650 integrated circuits were used in the assembly of the converter. The digital circuitry was mounted on wire stitch or wire wrap boards. Many of the more complex control functions were first wire wrapped to facilitate design changes prior to wire stitching of the final design. The circuitry employing linear elements, namely the Sync Generator, Video Mixer, and Color Generator, was fabricated on custom printed circuit boards. A total of 17 circuit boards, 17.5 by 25 cm (7 by 10 inches), were required and were housed in a commercially available ATR airborne enclosure. Typical wire stitch circuit boards are shown in Figure 16 and the custom printed circuit boards in Figure 17. The entire converter is shown in Figure 18. The front panel includes video, synchronization, test signals, a power connector, and electrical connections data and control signals from the SKC Computer. A forced air inlet port for cooling air is shown in the lower right-hand corner.

6. TEST RESULTS

As originally designed, the converter hardware was successfully tested in the laboratory. However, due to changes in the overall project requirements and inherent delays in developing the software, a temporary CPU (TCPU) was designed to provide an interface with the SKC computer and provide a subset of control functions in the absence of the full microprocessor based CPU. The TCPU is described fully in the companion report, AVRADCOM TR 80-E-4.

The converter using the TCPU has been successfully operated in the laboratory for many months in a display system test setup similar to Figure 1. The data for the terrain maps and elevation contours was generated by the computer. The symbology was generated by the external avionics symbol generator and fed to the Video Mixer in the converter, which insets the symbology into the terrain map background. Figure 19 is a picture of a terrain elevation map in 8 SOG with elevation contours and avionics symbology. Figures 20 to 23 show elevation maps in 16 SOG with and without various combinations of contours and symbology. Figure 24 shows the avionics symbology separately on a black background. Representative pictures from the 8 SOG sliding video mode are shown in Figures 25, 26, and 27.

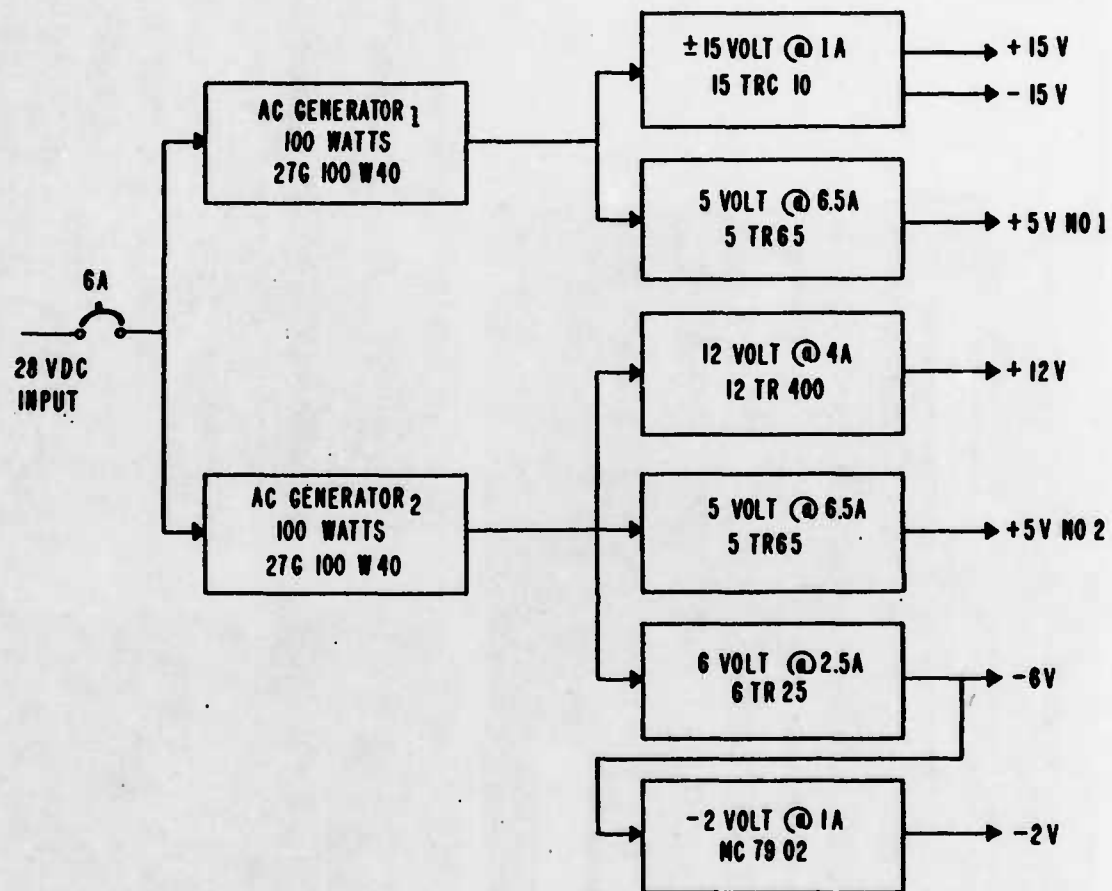


Figure 15. Block Diagram of Power Supply.

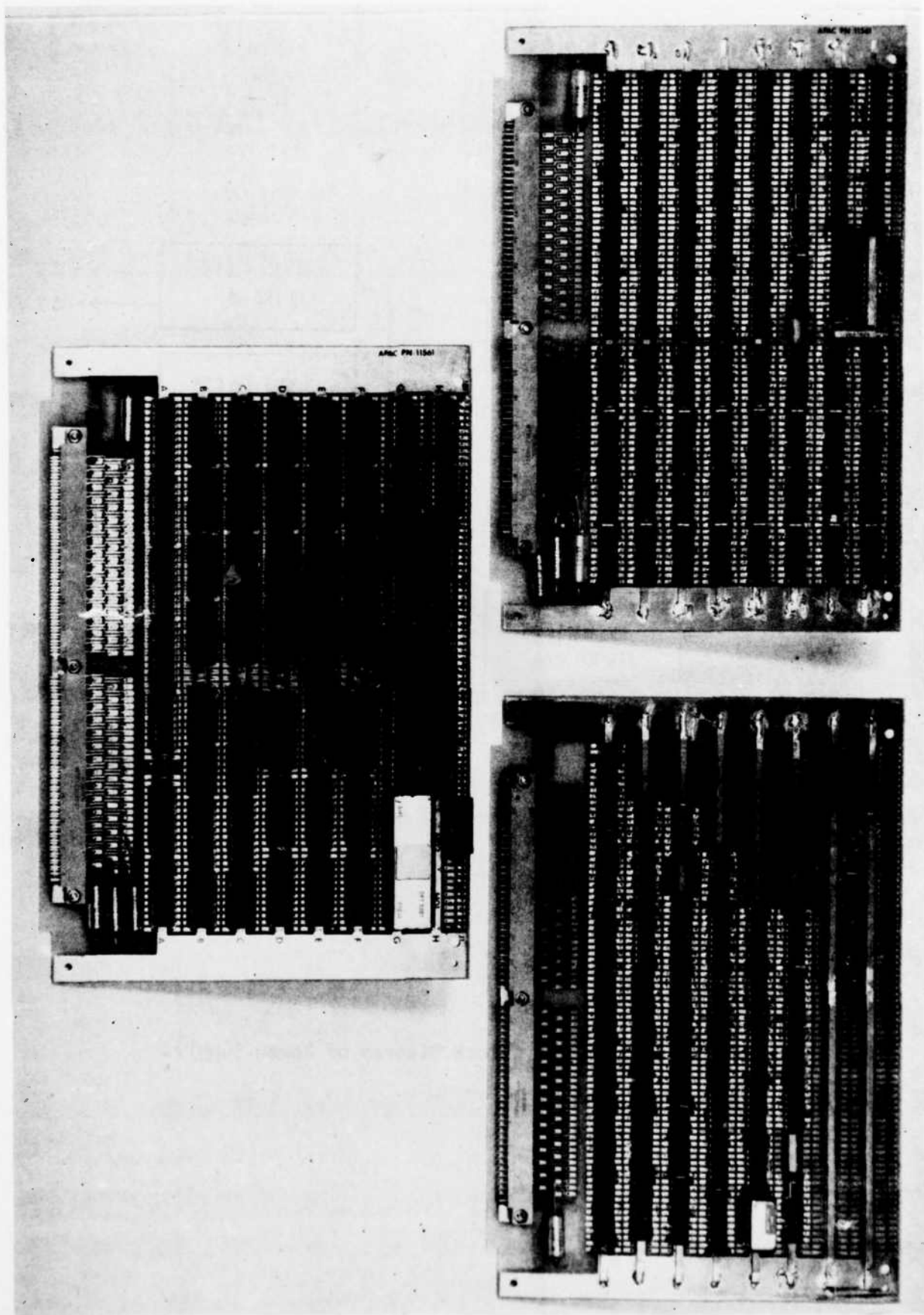


Figure 16. Typical Wire Stitch Circuit Boards.

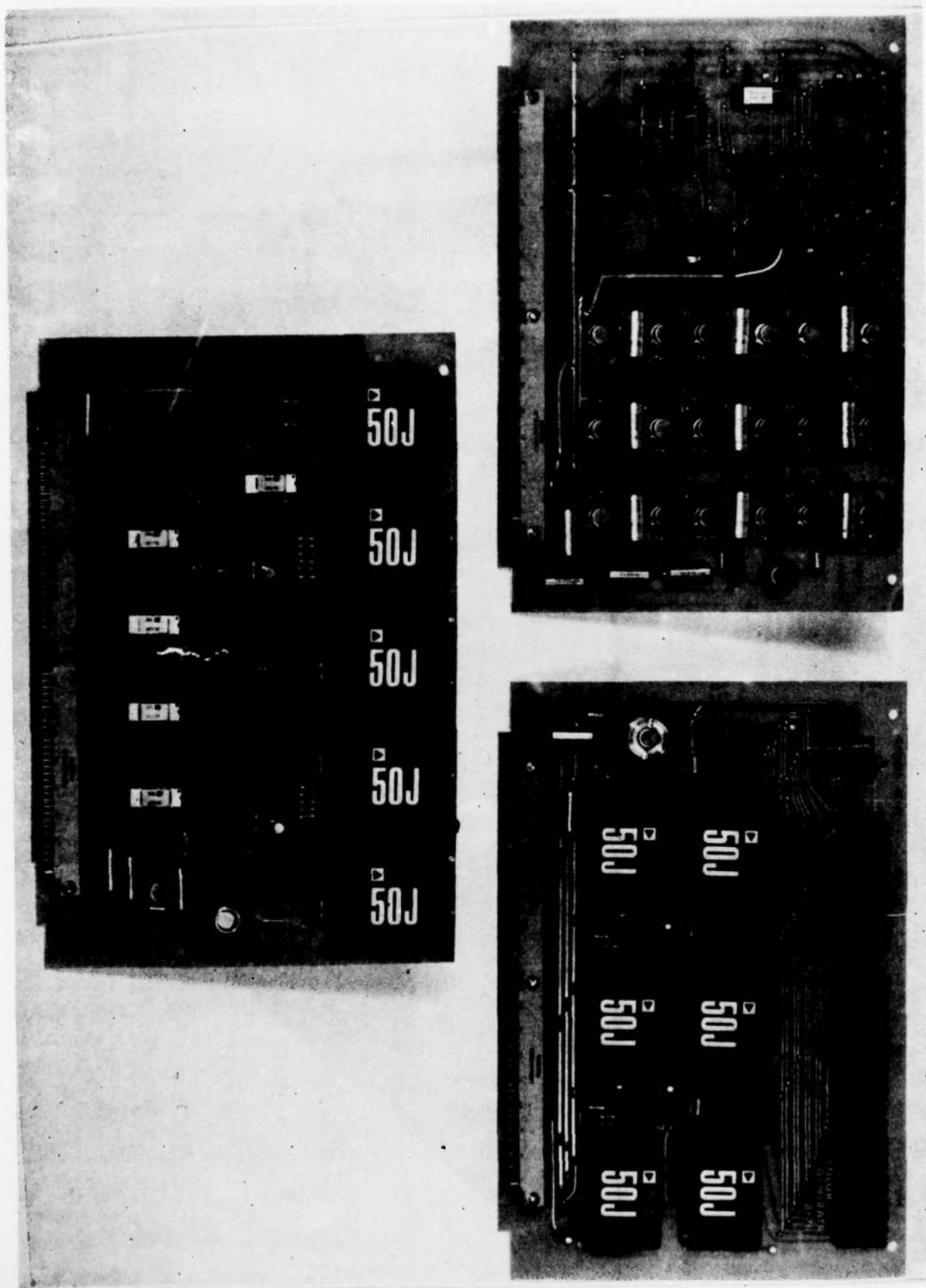


Figure 17. Custom Printed Circuit Boards.

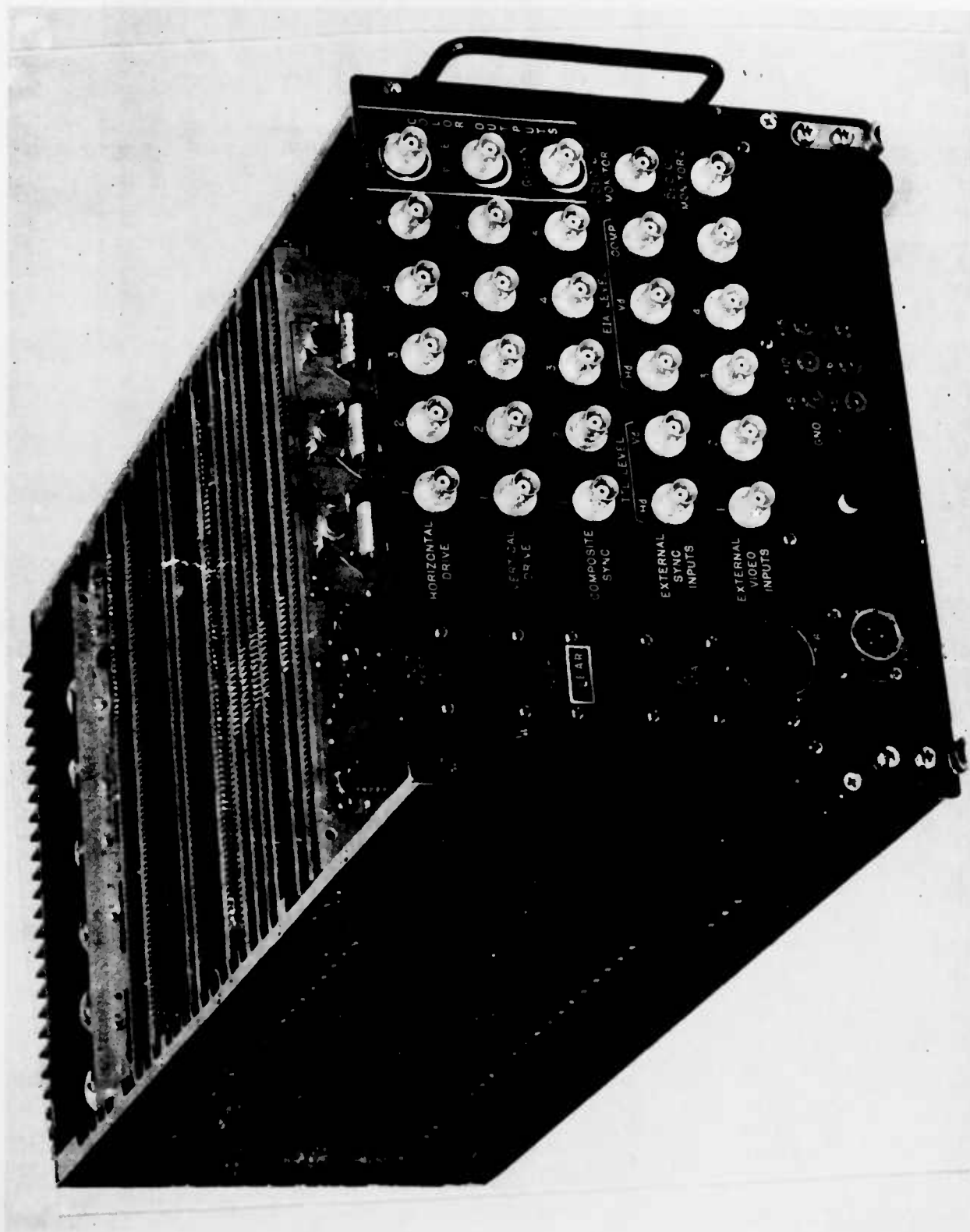


Figure 18. Digital to Video Converter.



Figure 19. Elevation Map in 8 Shades-of-Grey with Contours and Symbolology.



Figure 20. Elevation Map in 16 Shades-of-Grey.

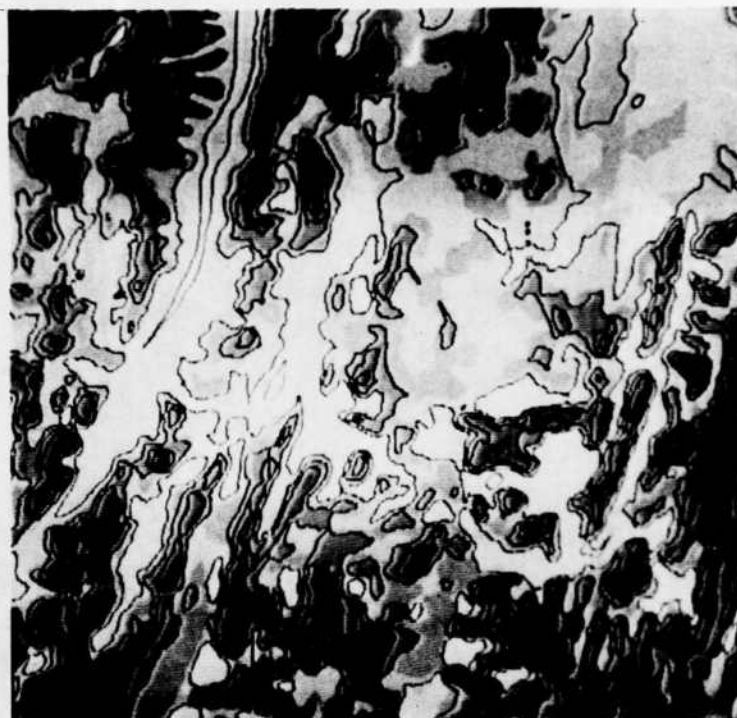


Figure 21. Elevation Map in 16 Shades-of-Grey with Contours.

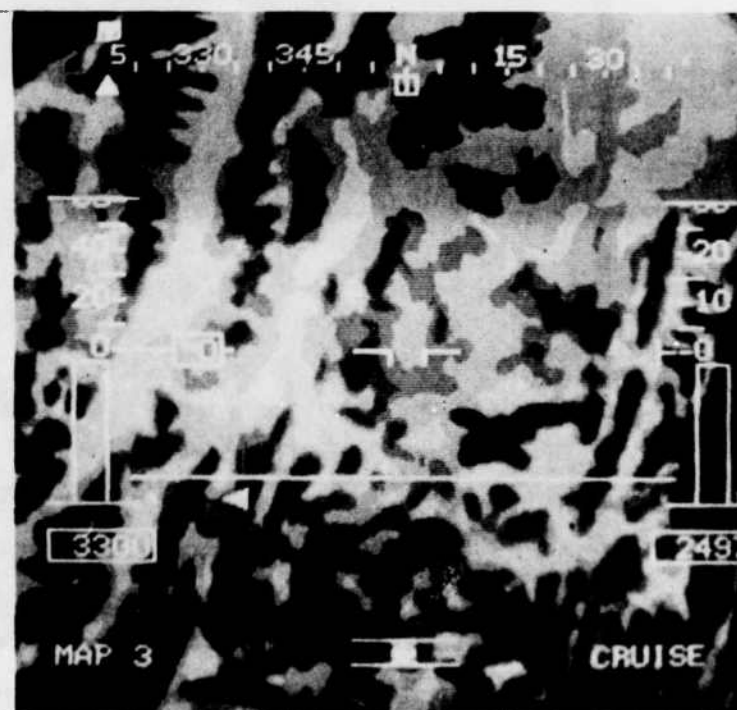


Figure 22. Elevation Map in 16 Shades-Of-Grey with Symbolology.

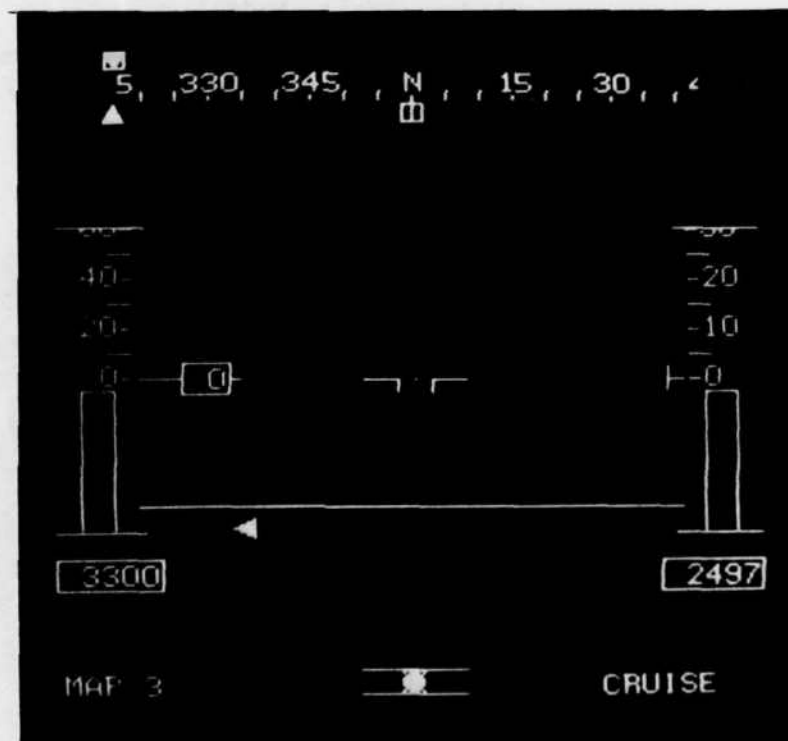
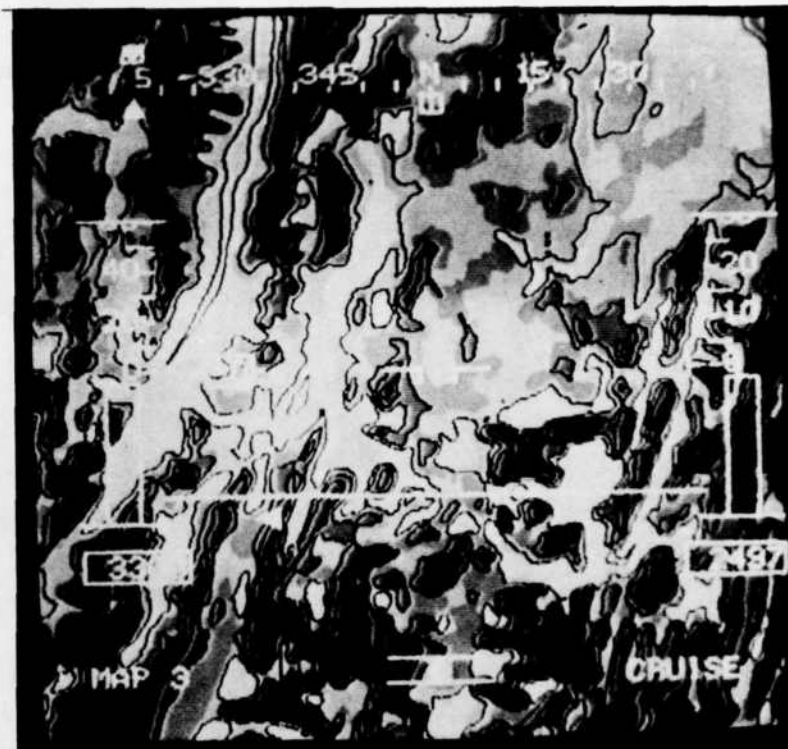


Figure 24. Avionics Symbology.

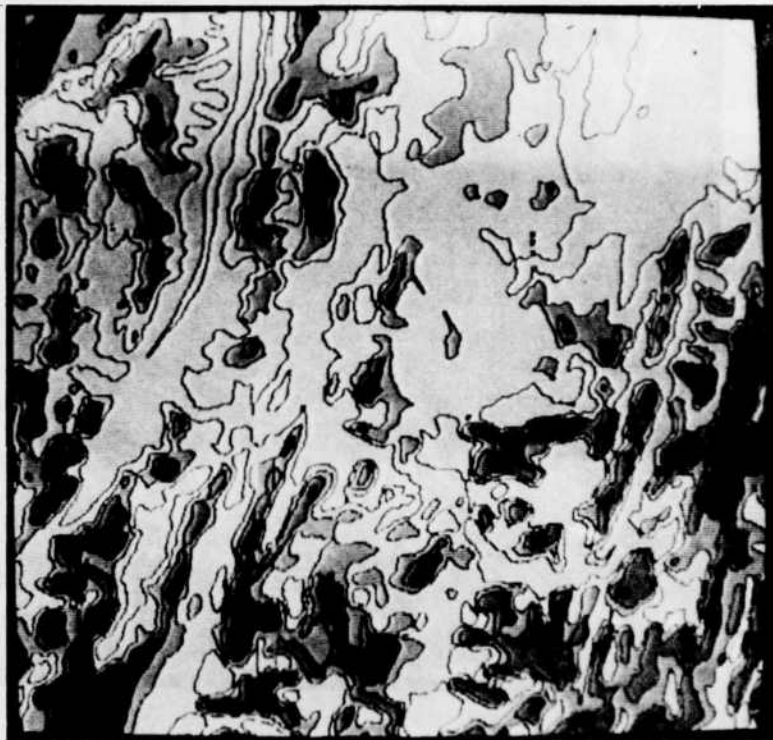


Figure 25. Elevation Map in 8 Shades-of-Grey Sliding Scale, Mode 1.

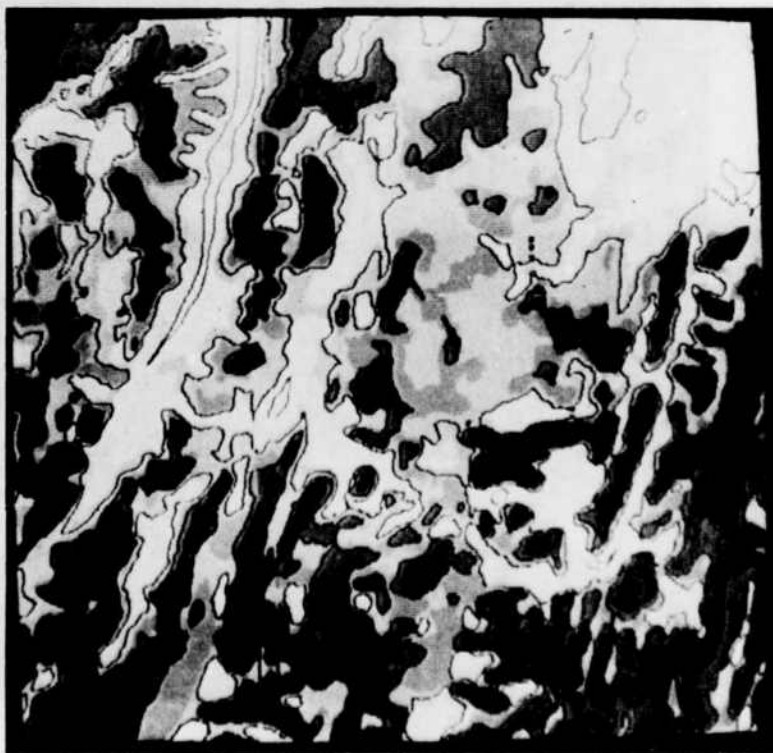


Figure 26. Elevation Map in 8 Shades-of-Grey Sliding Scale, Mode 3.

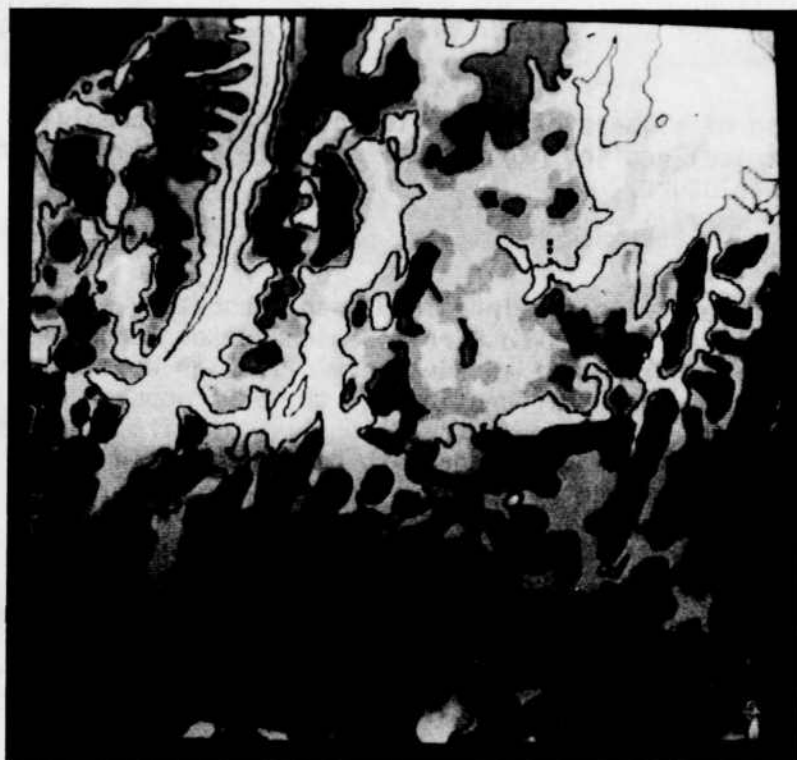


Figure 27. Elevation Map in 8 Shades-of-Grey
Sliding Scale, Mode 6.

The converter has also been operating for several months in the AVRADA UH-60 STAR helicopter to demonstrate the concept of nap-of-the-earth flight and navigation with a digitally generated map.

7. CONCLUSIONS

The programmable converter developed under this program provides a wide variety of formats for map, flight symbol, and alphanumeric character presentation. It also provides external video mixing and synchronization capability for the evaluation of numerous night navigation, pilotage, and nap-of-the-earth flight techniques. This display versatility was not available in previous hard-wired converters used for these studies.

The extensive use of high-level integrated electronic technologies made feasible the converter's electrical design, programmable operation, and packaging within an acceptable airborne enclosure.

8. FUTURE PLANS

As a result of the experience gained from both laboratory simulation and actual flight test, a contract was awarded to Harris Semiconductor Corporation (Contract No. DAAK-80-80-C-0780) for the design of an advanced full color digital moving map generator, combining the computational functions of the SKC computer and the converter into one box for use in the laboratory. Additionally, an airborne unit is being developed under a joint Army/Air Force program to be demonstrated in the Army UH-60 STAR helicopter and the Air Force F-16 AFTI aircraft.

9. ACKNOWLEDGEMENTS

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